

Understanding Switched Capacitor Analog Blocks

By: Dave Van Ess

Associated Project: Yes

Associated Part Family: CY8C25xxx, CY8C26xxx

Summary

The versatility of system design on the PSoC™ microcontroller relies on switched capacitor analog blocks. This paper will explain the theory of their operation and provide practical examples of their application.

Introduction

Analog circuit design most often requires the use of resistors, capacitors, and integrated active devices. It is the nature of integrated circuitry that small, accurate resistors are harder to build and more expensive than capacitors. Given that making capacitors is easier and cheaper, it follows that techniques would be developed to use capacitors to build accurate analog circuitry. These techniques lead to switched capacitor (SC) architectures that control the movement of charge between capacitors with the precise timing of switches, instead of relying on resistors to move current from one node to another. Numerous texts have been written on this subject. This Application Note provides:

- A brief tutorial on switched capacitor techniques.
- A detailed description of the switched capacitor PSoC blocks.
- Examples of practical circuits using these blocks.

It's All About Moving Charge

Analog circuit design is all about controlling the movement of charge between voltage nodes. Figure 1 shows charge movement through a resistor and through a switched capacitor.

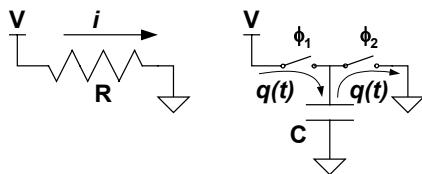


Figure 1: Moving Charge with Current Stimulus

Equation (1) shows the current flow from a voltage potential to ground through the resistor shown in Figure 1:

$$i = \frac{V}{R} \quad (1)$$

This current is a linear, continuous movement of charge.

When the ϕ_1 switch is closed and the ϕ_2 switch is open, the capacitor charges to the full potential. The equation of the charge stored is:

$$q = CV \quad (2)$$

When the ϕ_1 switch is opened and ϕ_2 switch is closed, all this stored charge moves to ground. For each precise sequential pair of switch closures, a quantum of charge is moved. If these switches are controlled at the rate of f_s , the charge quanta also move at this rate. Equation (3) shows that the repetitive movement of charge is a current:

$$i = q/t = f_s q = f_s CV \quad (3)$$

Unlike the case of the resistor, this current is not a continuous movement of charge. The charge moves in clumps (quanta). This is not a problem for a sampled system where the signal is sampled at the end of each sample cycle. Equation (4) shows that a switched capacitor is equivalent to a resistor when they have equivalent ratios of voltage drop verses delivered current:

$$\frac{V}{i} = R = \frac{1}{f_s C} \quad (4)$$

The equivalent resistance is inversely proportional to the capacitance and the switching frequency. The relative value of the resistance can be altered, merely by changing the switching frequency. The larger “C” is, the larger the charge quanta. This means more current and a smaller equivalent resistance. Making “ f_s ” bigger causes more quanta to be transferred per unit time. Again, this means a higher current and lower effective resistance.

Here are the timing requirements for ϕ_1 and ϕ_2 :

- Never close the ϕ_1 and ϕ_2 switches at the same time.
- Give the ϕ_1 switch time to open before closing the ϕ_2 switch.
- Give the ϕ_2 switch time to open before closing the ϕ_1 switch.
- When selecting a sampling rate, allow enough time for the circuitry to fully charge and discharge in the allotted phase cycle.

Active Switched Cap Circuits

It's okay to shuffle charge but most circuits require gain. Figure 2 shows a simple architecture for a fixed gain amplifier. It consists of an opamp, an input capacitor (C_A), a feedback capacitor (C_F), and 5 switches:

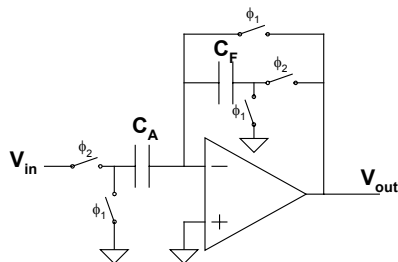


Figure 2: A Switched Cap Fixed Gain Amplifier

This circuit has two distinct phases to its operation:

- ϕ_1 The acquisition of signals
- ϕ_2 The transfer of charge

Figure 3 shows that three switches are closed during the signal acquisition (ϕ_1) phase.

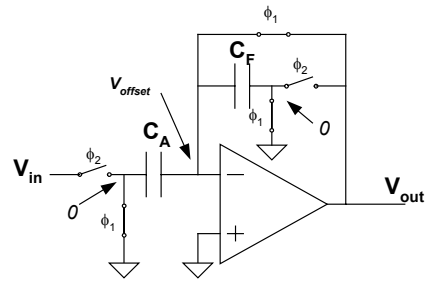


Figure 3: Set for Signal Acquisition (ϕ_1) Phase

The opamp is configured as a follower. Negative feedback causes the voltage at the inverting input to be ground. It's actually going to be a bit off. The deviation from zero is the opamp's input offset error (V_{offset}). The input side of C_A is set to ground, as is the output side of C_F . Measurement of this offset error and storage on both capacitors removes the effect this offset error may have on the output during the charge transfer phase. Since this measurement is done automatically during the acquisition phase, it is known as an “autozero” adjustment.

For a transition period between the phases, all the switched are open. This period is brief and the charge stored on the capacitors does not change.

Figure 4 shows that two switches are closed during the charge transfer (ϕ_2) phase:

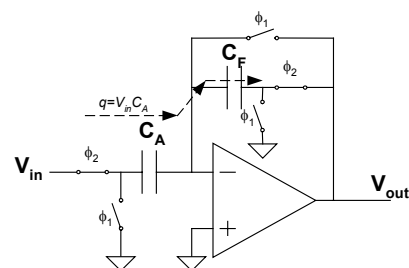


Figure 4: Set for Charge Transfer (ϕ_2) Phase

Equation (5) defines the amount of charge needed to charge the input capacitor now that its input has been connected to V_{in} :

$$q = V_{in} C_A \quad (5)$$

This charge has no other path to take except through the feedback capacitor. Therefore, the feedback capacitor must receive the same charge transfer. Equation (6) describes how much the output voltage will change due to this charge transfer:

$$V_{out} = -\frac{q}{C_F} \quad (6)$$

Equation (7) combines Equations (5) and (6) to produce the transfer function for this amplifier:

$$Gain = \frac{V_{out}}{V_{in}} = -\frac{C_A}{C_F} \quad (7)$$

The result is an inverting amplifier with a gain set by the ratio of its two capacitors.

Please note that the output voltage is available after the transfer of charge. The output voltage is near ground (V_{offset}) during the signal acquisition.

Theme and Variation

Figure 5 appears to be an exact copy of Figure 2. A closer examination shows that the input switches have swapped phase:

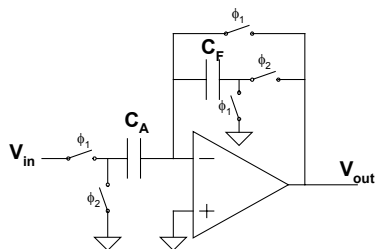


Figure 5: Amplifier with Input Switches Swapped

Now the input capacitor acquires V_{in} during the acquisition phase. The charge needed to pull the input back to ground during the transfer phase moves in the opposite direction to that of the first example. This causes the output voltage to also move in the opposite direction. The result is a positive gain amplifier with a gain defined in Equation (8):

$$Gain = \frac{V_{out}}{V_{in}} = \frac{C_A}{C_F} \quad (8)$$

Figure 6 shows the modification that allows the correct phasing for both positive and negative gain operation.

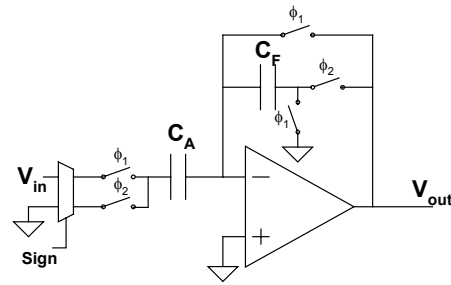


Figure 6: Selectable Gain Polarity Amplifier

For the rest of these examples the “Sign” is assumed to be positive. That is, the C_A acquires V_{in} during ϕ_1 and moves back to zero during ϕ_2 .

Comparator

Figure 7 shows a modification where the switch in series with the feedback capacitor is removed:

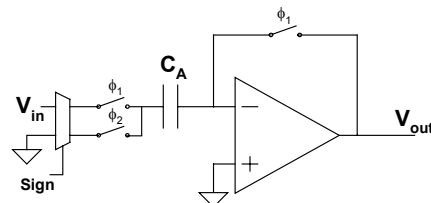


Figure 7: A Comparator

This removes the capacitor from the feedback loop, effectively setting its value to zero. Equation 8 states amplifiers gain to be the ratio of the two capacitors. If the feedback capacitor is removed then the gain is infinite and the amplifier acts like a comparator.

Integrator

Figure 8 shows that with the switch to zero, the feedback capacitor as been removed:

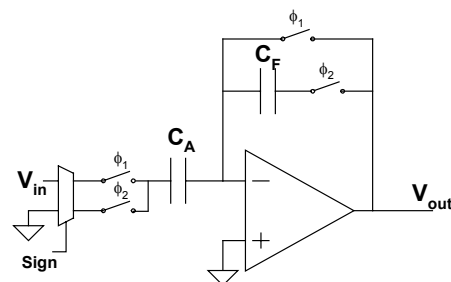


Figure 8: An Integrator

This keeps the charge on the feedback capacitor from being removed during the acquisition phase while still allowing the transfer of the input charge. Equation (9) defines its operation:

$$V_{out} = V_{out} z^{-1} + V_{in} \frac{C_A}{C_F} \quad (9)$$

Manipulating Equation 9 results in the transfer Equation (10):

$$Gain = \frac{V_{out}}{V_{in}} = \frac{C_A}{C_F} \frac{1}{(1 - z^{-1})} \cong \frac{1}{s} \left(f_s \frac{C_A}{C_F} \right) \quad (10)$$

If while examining Equations (9) and (10) you find you don't have a clue what's going on, don't panic. They basically state that this circuit is an integrator. On the other hand if these equations make sense, then you will see that this is an adjustable integrator that can be varied by changing the capacitor ratios or adjusting the sampling frequency.

Differentiator

Figure 9 shows that input is permanently connected to the input capacitor:

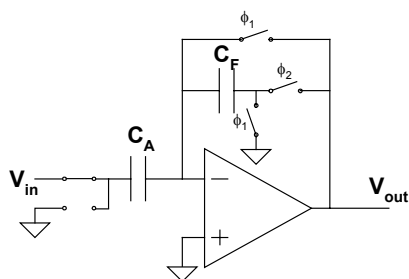


Figure 9: A Differentiator

This topology makes the feedback capacitor act like a resistor and input capacitor act like a capacitor. Circuitry that allows a capacitor to look like a capacitor, imagine that! As odd as it may seem it does allow for operation shown in Equation (11):

$$(V_{in} - V_{in} z^{-1}) \cdot C_A = -V_{out} C_F \quad (11)$$

Manipulating Equation (11) results in the transfer Equation (12):

$$Gain = \frac{V_{out}}{V_{in}} = -(1 - z^{-1}) \frac{C_A}{C_F} \cong -s \left(\frac{1}{f_s} \frac{C_A}{C_F} \right) \quad (12)$$

Equation (12) shows that this is an adjustable differentiator.

What's So Special About Ground?

So far, all the examples have the input voltage referenced to ground. Ground may be a convenient reference point but others are possible. Figure 10 show the standard circuit with an improved reference selection:

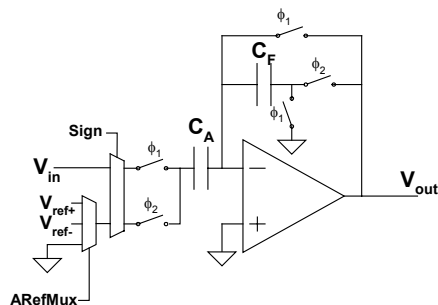


Figure 10: Improved Reference Selection

ARefMux allows for the selection of two other references besides ground. Equation (13) defines the output voltage for an amplifier. The equations are for the cases where the reference is ground, V_{ref+} , or V_{ref-} :

$$\begin{aligned} V_{out} &= \frac{C_A}{C_F} V_{in} \\ V_{out} &= \frac{C_A}{C_F} (V_{in} - V_{ref+}) \quad (13) \\ V_{out} &= \frac{C_A}{C_F} (V_{in} - V_{ref-}) \end{aligned}$$

Combining the comparator in Figure 7 with the reference selection in Figure 10 results in a comparator with multiple compare points shown in Figure 11:

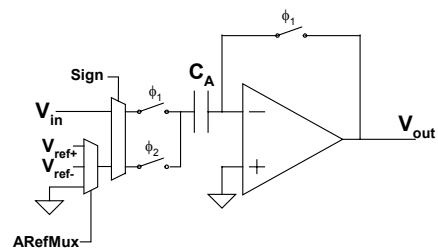


Figure 11: Poor Man's 2 Bit ADC

With proper control of ARefMux it is possible to determine if V_{in} is:

- Greater than V_{ref+}
- Less than V_{ref+} but greater than ground
- Less the ground but greater than V_{ref-}
- Less than V_{ref-}

These four states make this circuit a two-bit analog to digital converter (ADC). (Whether “two bit” means four levels, or “cheap and trivial” is an exercise left the reader.)

Real Analog to Digital Conversion

Slight modification of the reference selection allows this circuit to function as an analog to digital modulator. Figure 12 shows that a comparator has been added to the output and is connected to the reference selection mux:

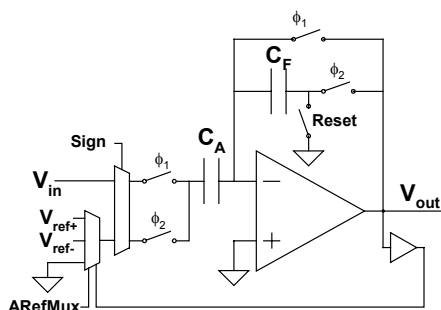


Figure 12: Analog to Digital Modulator

Selecting the proper ARefMux value allows the output of the comparator to determine the reference voltage. The relationship is:

- The reference is set to V_{ref+} when the comparator is high (positive output value).
- The reference is set to V_{ref-} when comparator is low (negative output value).

The switches around the feedback capacitor are configured to make an integrator. The comparator control causes a reference, with the same polarity as the V_{out} , to be subtracted from the input. This negative feedback attempts to move the V_{out} back towards zero. Equation (14) describes V_{out} , given:

- The initial condition of V_{out} is zero.
- The switch cycle is preformed “ n ” times.
- V_{out} is greater than zero (comparator is high) “ a ” of those times.

$$V_{out} = \frac{C_A}{C_F} n V_{in} - \frac{C_A}{C_F} a V_{ref+} - \frac{C_A}{C_F} (n - a) V_{ref-} \quad (14)$$

Given that the references are of equal but opposite polarity, solving for V_{in} results in Equation (15):

$$V_{in} = V_{ref} \frac{(2a-n)}{n} + \frac{1}{n} V_{out} \frac{C_F}{C_A} ; (V_{ref} = V_{ref+} = -V_{ref-}) \quad (15)$$

V_{in} is a function of V_{ref} and V_{out} . As stated earlier, the negative feedback causes V_{out} to move back towards ground every cycle. This makes V_{out} less than $(C_A/C_F) * V_{ref}$. As “ n ” becomes larger, the contribution of V_{out} to Equation (15) becomes negligible. This allows for a more simplified Equation (16):

$$V_{in} = V_{ref} \left(\frac{2a}{n} - 1 \right) ; \left(\frac{1}{n} V_{out} \frac{C_F}{C_A} < \frac{1}{n} V_{ref} \approx 0 \right) \quad (16)$$

V_{in} is not dependent on the ratio of the two capacitors. It is only a function of V_{ref} , and the ratio of “ a ,” and “ n .” Measuring V_{in} is just a function of counting the number of times the comparator is high (“ a ”) during a sequence of “ n ” switch cycles. The range is $-V_{ref}$ ($a = 0$) to $+V_{ref}$ ($a=n$) and the resolution is $2V_{ref}/n$. The longer the period (larger “ n ”), the better the resolution of the voltage measurement.

Switched Capacitor PSoC Blocks

The architecture discussed is quite versatile. It allows for many different functions merely by altering the circuit’s switch closures. This architecture is used as the basis for the switched capacitor blocks in the PSoC microcontroller and is implemented with Type A and Type B Switched Capacitor Blocks. There are small differences exist between the block types.

Type A Switched Capacitor Blocks

Figure 13 shows the type A switched capacitor block. A larger copy of this diagram along with a map of the Control registers for the block can be found in [Appendix A](#).

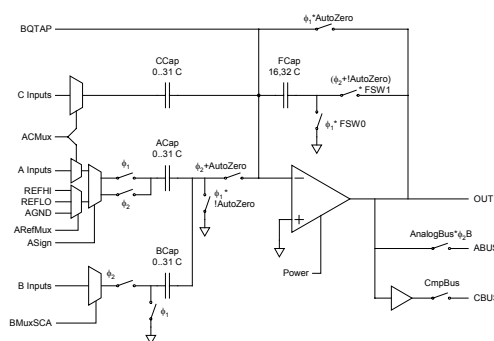


Figure 13: Type A Switched Capacitor Block

Figure 13 looks a lot like the final architecture shown in Figure 12 with the following additions:

- A programmable **CCap** capacitor connects to the summing node of the opamp.
- A programmable **BCap** switched capacitor connects to the summing node of the opamp.
- An **AnalogBus** switch connects the opamp's output to an analog buffer.
- A **CompBus** switch connects the comparator to the digital blocks.

The **BCap** acts many ways like the **ACap** except that it only samples its input on ϕ_2 and is always referenced to ground. It is primarily used for multiple input amplifiers. The **CCap** primary benefits filter design. A larger copy of Figure 13 along with a map of the four registers that control its operation is shown in [Appendix A](#).

One Block, 15 Parameters

There are 15 different parameters for a type A switched cap block. They are shown below with a description of its operation:

- **FCap**
A one-bit field to set the value of FCap to either 16 or 32 units. Each unit of capacitance is approximately 50 femto farads.
- **ClockPhase**
A one-bit field that, when set, swaps the ϕ_1 and ϕ_2 phases. It is primarily used to match the input signal sampling to the output of a switched cap block.
- **ASign**
A one-bit field to set the gain of the block to either positive or negative.
- **ACap**
A five-bit field to set the value of ACap from 0 to 31 units.
- **ACMux**
A three-bit field to select the inputs to the ACap and the CCap. Appendixes [C](#) and [D](#) show the connection options.
- **BCap**
A five-bit field to set the value of BCap from 0 to 31 units.
- **AnalogBus**
A one-bit field that, when set, connects the output to an analog buffer.

- **CompBus**
A one-bit field that, when set, connects the comparator to the data inputs of the digital blocks.
- **AutoZero**
A one-bit field that, when set, forces an autozero during the ϕ_1 signal acquisition phase.
- **CCap**
A five-bit field to set the value of CCap from 0 to 31 units.
- **ARefMux**
A two-bit field to select the voltage potential that the A input is referenced to. It can be AGND, V_{ref+} , V_{ref-} , or a voltage reference determined by the state of the output comparator.
- **FSW1**
A one-bit field to select if FCap is connected. If low FCap is not connected, the circuits function as a comparator. If set, the FCap is in the feedback path so the circuit functions as a gain stage or integrator.
- **FSW0**
A one-bit field to select if FCap is discharged during ϕ_1 . If set to one, the FCap is discharged and the circuit functions as a gain stage. If set to zero, the capacitor is not discharged and the circuit functions as an integrator.
- **BMux(SCA)**
A two-bit field to set the inputs to the BCap. [Appendix E](#) shows the connection options.
- **Power**
A two-bit field to set the power for the block. It can be off, low, medium, or high.

Type B Switched Capacitor Blocks

Figure 14 shows the type B switched capacitor block. A larger copy of this diagram along with a map of the Control resistors for the block can be found in [Appendix B](#).

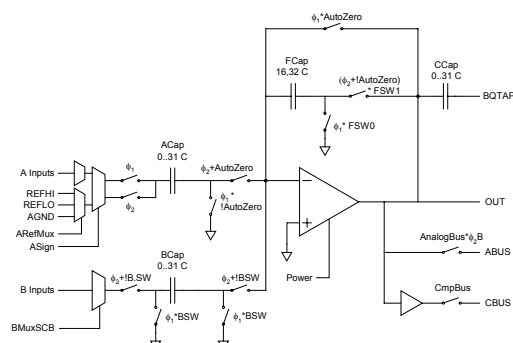


Figure 14: Type B Switched Capacitor Block

Figure 14 looks a lot like the type A SC block shown in Figure 13 with the following differences:

- There is no longer a multiplexed input to **CCap** but a connection to the output of the block. The other side of **CCap** connects to the summing node of the type A SC block next to it. It is used to build biquad filters.
- The control field **BSW** allows **BCap** to function as either a switched capacitor or as just a capacitor.
- A programmable **BCap** switched capacitor connects to the summing node of the opamp.
- An **AnalogBus** switch connects the opamp's output to an analog buffer.
- A **CompBus** switch connects the comparator to the digital blocks.

The BCap acts many ways like the ACap except that it only samples its input on ϕ_2 and is always referenced to ground. It is primarily used for multiple input amplifiers. The CCap primary benefits filter design.

One Block, 16 Parameters

There are sixteen different parameters for a type B switched cap block. Thirteen are common with the type A SC block and have already been discussed. The remaining three are shown below along with a description of operation:

- **AMux**
A three-bit field to set the inputs to the ACap. [Appendix C](#) shows the connection options.
- **BSW**
A one-bit field when selected causes **BCap** to function as a switched capacitor input. If not set then it functions as a capacitor.
- **BMux(SCB)**
A one-bit field to set the inputs to the BCap. [Appendix E](#) shows the connection options.

SC Blocks and PSoC Architecture

Figure 15 shows the array of analog PSoC blocks for the CY8C25xxx/CY8C26xxx family of parts.

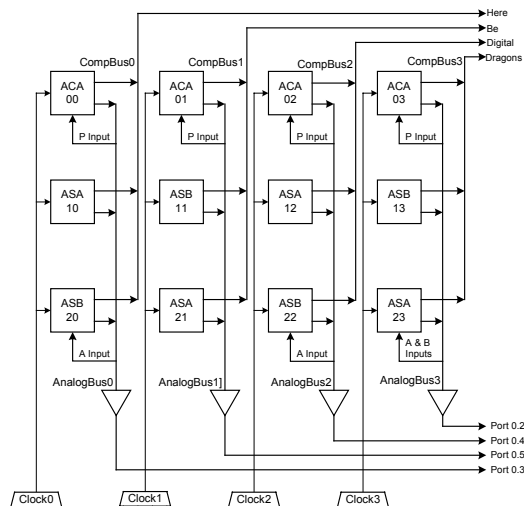


Figure 15: The Analog PSoC Blocks

There are four columns of blocks with each column having its own analog bus, comparator bus, and clock to generate the ϕ_1 and ϕ_2 clocks. Each column contains one type "A" SC block and one type "B" SC block for a total of eight SCBlocks.

Different User Modules use different numbers of blocks. For example:

- A **DAC6** uses one SC block.
- A **DAC8** uses two SC blocks.
- **DELSIG8**, **DELSIG11**, and **ADCINC12** ADCs each use only one SC block.
- **LPF2** uses two SC blocks.
- A **PWM8** is a digital only User Module and uses no SC blocks.

Presently there are many more applications for the SC blocks than User Modules. To assist the user, a fully parameterized SC block User Module has been developed.

PSoC SCBlock User Module

The SCBlock User Module can be found under the Generic title of the User Module selections. This is the left most area of the User Module Selection View. Figure 16 shows the icon:

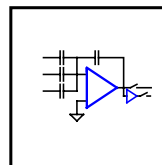


Figure 16: Icon for the SCBLOCK User Module

This block can be placed in any of the eight available SB blocks. Placement allows users to select all SC parameters.

Cool Applications

The SC blocks are very versatile allowing for many unique applications. Some are shown below. A copy of the project containing all three examples associated with this Application Note is available on our web site.

Example 1: Differential Amplifier with Common Mode Output

Figure 17 shows the architecture for a differential amplifier with a common mode output:

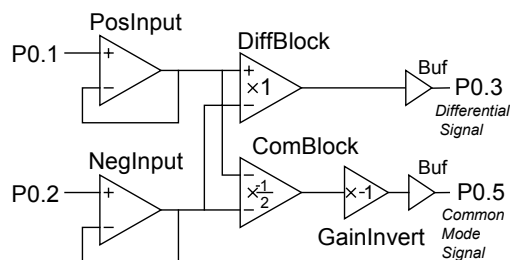


Figure 17: Differential Amplifier with Common Mode Output

A common mode output signal is useful to many signal processing applications. It is also highly useful where common mode feedback is used to drive a shield or signal guard. The PSoC implementation is shown in Figure 18:

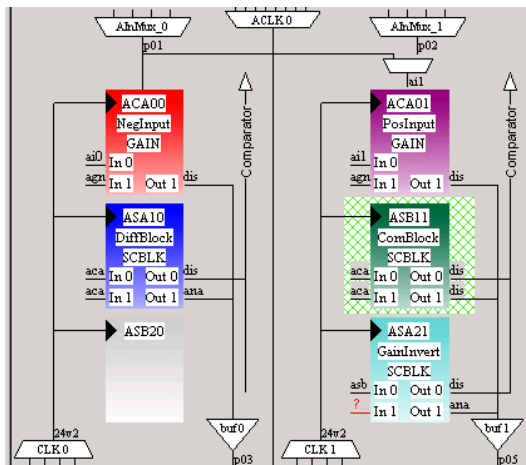


Figure 18: PSoC Block Placement of Differential Amplifier with Common Mode Output

The two input buffers are PGA User Modules with matched gains.

The difference output is defined by Equation (17):

$$V_{\text{difference}} = \text{PosInput} - \text{NegInput} \quad (17)$$

The amplifier is an A -B amplifier with a gain of one. Its parameters are shown in Figure 19:

User Module Parameters	
FCap	16
ClockPhase	Norm
ASign	Pos
ACap	16
ACMux	ACA01
BCap	16
AnalogBus	AnalogOutBus_0
CompBus	Disable
AutoZero	On
CCap	0
ARefMux	AGND
FSW1	On
FSW0	On
BMux	ACA00
Power	High

Figure 19: Parameters for DiffBlock SCBLOCK

For a difference amplifier with a gain of one, the values of **FCap**, **ACap**, and **BCap** must be the same. **CCap** is not used so its value is set to zero. The continuous time blocks source both input signals so that there is no phasing problem with sampling their outputs. **ClockPhase** can remain set to "Norm." The **ACMux** is set to connect its input to "ACA01." **ARefMux** is set to "AGND" so both input references have the same potential. **BMux** is set to connect its input into "ACA00." **ASign** is set to "Pos." To be an amplifier, **FSW1**, **FSW0**, and **AutoZero** must be set "On." The comparator is not used so **CompBus** is set to "Disable." **AnalogBus** is set to "AnalogOutBus0" so that the output can be brought to the analog buffer on P0[3]. **Power** is set "High."

The common mode output is defined by Equation (18):

$$V_{\text{common}} = \frac{\text{PosInput} + \text{NegInput}}{2} \quad (18)$$

What is desired is a stage that can implement an A+B amplifier. Unfortunately, the architecture limits the B input to negative gains. The solution is to build a -A-B amplifier and follow it with a gain stage of -1.

The parameters for a “- A - B” amplifier with a gain of $\frac{1}{2}$ are show in Figure 20:

User Module Parameters	
FCap	32
ClockPhase	Norm
ASign	Neg
ACap	16
AMux	ACA01
BCap	16
AnalogBus	Disable
CompBus	Disable
AutoZero	On
CCap	0
ARefMux	AGND
FSW1	On
FSW0	On
BSW	On
BMux	ACA00
Power	High

Figure 20: Parameters for the ComBlock SCBLOCK

For a gain of $\frac{1}{2}$ on both inputs, **FCap** is set to “32” and **ACap** and **BCap** are set to “16.” **CCap** is not used so its value is set to zero. The continuous time blocks source both input signals so that there is no phasing problem with sampling their outputs. **ClockPhase** can remain set to “Norm.” The **ACMux** is set to connect its input to “ACA01.” **ARefMux** is set to “AGND” so both inputs references have the same potential. **BMux** is set to connect its input into “ACA00.” **BCap** is required to be a switched capacitor so **BSW** is set “On.” **ASign** is set to “Neg.” To be an amplifier, **FSW1**, **FSW0**, and **AutoZero** must be set “On.” The comparator is not used so **CompBus** is set to “Disable.” **AnalogBus** is also not used so it is set to “Disable.” **Power** is set “High.”

This block is to be followed by a gain inversion stage. The parameters for a -1 gain stage are shown in Figure 21:

User Module Parameters	
FCap	16
ClockPhase	Norm
ASign	Pos
ACap	16
ACMux	ASB11
BCap	0
AnalogBus	AnalogOutBus_1
CompBus	Disable
AutoZero	On
CCap	0
ARefMux	AGND
FSW1	On
FSW0	On
BMux	?
Power	High

Figure 21: Parameters for the GainInvert SCBLOCK

For a gain of -1, the values of **Fcap** and **ACap** must be the same. **BCap** and **CCap** are not used so their values are set to zero. **ASign** is set to “Neg.” Its input is sampled on the same phase as a valid Com Block output signal so **ClockPhase** can remain set to “Norm.” The **ACMux** is set to connect its input to “ASB11.” **ARefMux** is set to “AGND.” **BMux** is not needed so it is not set. Again **FSW1**, **FSW0**, and **AutoZero** must be set “On.” The comparator is not used so **CompBus** is set to “Disable.” **AnalogBus** is set to “AnalogOutBus1” so that the output can be brought to the analog buffer on P0[5]. **Power** for this example is set “High.” The actual setting for other applications is determined by signal bandwidth.

These five blocks implement the circuit shown in Figure 17. The columns clocks are set to 1 MHz. This sets the sample rate to 250 Ksps. It is recommended that when used as amplifiers, the SCBlocks should not be sampled faster than 350 Ksps.

Example 2: A Two-Bit ADC

Way back in Figure 12, a four state ADC was shown using an SCBlock as a comparator and changing the references to determine four different conditions. Figure 22 shows the architecture:

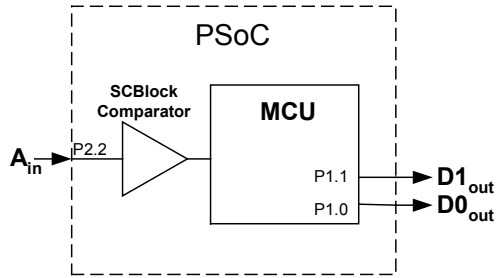


Figure 22: SCBlock Comparator

The PSoC implementation is shown in Figure 23:

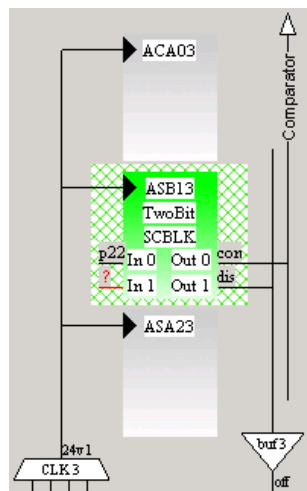


Figure 23: PSoC Block Placement of TwoBit ADC

The input is brought in from P2[2] and to a SCBlock (**TwoBit**). It is configured as a comparator. Software manipulates the **ARefMux** field in Control register **TwoBit_SCBLOCKcr3** to select the reference to be V_{ref+} , V_{ref-} , or V_{ref} .

Bit 7 of the **Analog Comparator Control Register (CMP_CR)** allows the software to determine the state of the column 3 comparator. This allows the software to determine if the input is:

- Greater than V_{ref+}
- Less than V_{ref+} but greater than ground
- Less than ground but greater than V_{ref-}
- Less than V_{ref-}

The parameters for a comparator with a configurable reference are shown in Figure 24:

User Module Parameters	
FCap	16
ClockPhase	Norm
ASign	Pos
ACap	31
AMux	Port_2_2
BCap	0
AnalogBus	Disable
CompBus	ComparatorBus_3
AutoZero	On
CCap	0
ARefMux	AGND
FSW1	Off
FSW0	Off
BSW	Off
BMux	?
Power	High

Figure 24: Parameters for the TwoBit SCBLOCK

For a comparator, the **FCap** is not connected so its value is unimportant. **ACap** needs to be some non-zero value. **BCap** and **CCap** are not used so their values are set to zero. The input is from a continuous input signal so there is no phase sampling problem and **ClockPhase** can remain set to "Norm." The **ACMux** is set to connect its input to "Port_2_2." **ARefMux** is to be controlled by software but is set to a default value of "AGND." **BMux** is not needed so it is not set. **ASign** is set to "Pos." To be a comparator **FSW1** and **FSW0** must be set to "Off," but **AutoZero** must be set "On." This disconnects the feedback capacitor. Setting **CompBus** to "ComparatorBus_3" allows the CPU access to the state of the comparator. **AnalogBus** is set to "Disable." **BSW** is not used and is set to "Off." **Power** is set "High." The column clock is set to 8 MHz. This sets the sample rate to 2 Msp/s. It is recommended that when used as a comparator, the SCBlocks should not be sampled faster than 2 Msp/s.

Code Example 1 shows the software used to control this application.

```

;-----
; Switched Capacitor
;
; This software sets up and controls the
; three examples for AN2041.
;
; Copyright (c) 2002 Cypress Microsystems
; Inc. All rights reserved.
;-----
export _main
include 'm8c.inc'
include 'ComBlock.inc'
include 'DiffBlock.inc'
include 'GainInvert.inc'
include 'NegInput.inc'
include 'PosInput.inc'
include 'TwoBit.inc'
include 'Buffer.inc'
include 'DigitalBuffer.inc'
include 'ADModulator.inc'

_main:
;-----
; code for example 1
;-----
mov A,PosInput_HIGHPOWER
call PosInput_Start
mov A,NegInput_HIGHPOWER
call NegInput_Start
mov A,Buffer_HIGHPOWER
;SCBlocks already on

;-----
; code for example 3
;-----
call Buffer_Start
mov A,0
;SCBlocks already on

;-----
; code for example 2
;-----
call DigitalBuffer_Start
;SCBlocks already on
loop:
//set ARefMux to Agnd
and reg[TwoBit_cr3],3fh
nop
nop
tst reg[COMP_CR], COMP_CR_COMP3
if1: jz else1;(signal > AGND)
//set to REHI
or reg[TwoBit_cr3],40h
nop
nop
tst reg[COMP_CR], COMP_CR_COMP3
if2: jz else2;(signal > REFHI)
// REFHI < input
or reg[PRT1DR],03h ;Dout = 11
jmp endif2
else2:;(signal < REFHI)
// REFI>input > AGND
mov A,reg[PRT1DR] ;Dout = 10
or A,02h
and A,~01h
mov reg[PRT1DR],A
endif2:
jmp endif1
else1:;(signal < AGND)
//set to Reflow
or reg[TwoBit_cr3],80h
nop
nop
tst reg[COMP_CR], COMP_CR_COMP3
if3: jz else3;(signal > REFLOW)
// RELOW> input >AGND
mov A,reg[PRT1DR] ;Dout = 01
or A,01h
and A,~02h
mov reg[PRT1DR],A
jmp endif3
else3:;(signal < REFFLOW)
// input < REFLOW
and reg[PRT1DR],~03h ;Dout = 00
endif3:
endif1:

```

```

endloop: jmp loop
ret

```

Code 1: Example 1

The program runs in a loop where the input is continuously sampled and compared with the selectable references to determine one of four different levels. D_{out1} and D_{out0} are set accordingly.

Example 3: Isolated Analog Driver

There are times where it is necessary to get an analog signal across an isolated barrier. For a higher frequency signal with no DC component, this can easily be done with capacitor or transformer coupling. For lower frequencies, the transformers and capacitors become increasing larger. The expense and size of these components for lower frequency and DC coupled signals makes this solution prohibitively expensive.

A cheaper solution requires using an SCBlock as an analog to digital (AD) modulator. Figure 12 shows an architecture for an AD Modulator that converts an input signal to a series of pulses where...

- A one represents V_{ref+}
- A zero represents V_{ref-}
- The average is equal to the input signal

Figure 25 shows how it can be assembled to pass the signal across an isolation barrier.

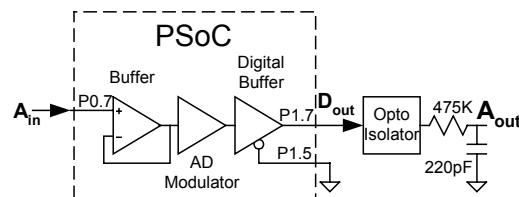


Figure 25: Isolated Analog Driver

The input signal (A_{in}) is buffered and passed to the AD Modulator where the signal is converted to a series of digital pulses. These pulses are brought out of the chip via the Digital Buffer. The pulses (D_{out}) pass through an Opto Isolator. Now isolated, these pulses are averaged to reconstruct an analog signal (A_{out}).

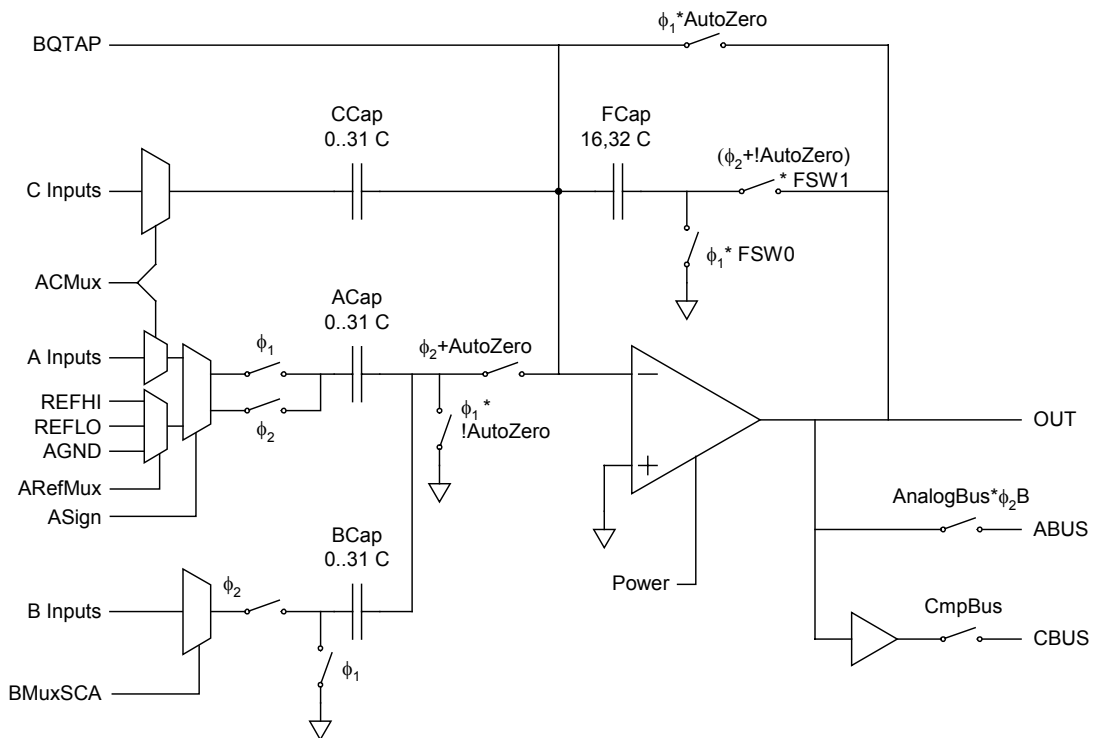
The low pass filter is set to 1.5 kHz to knock out the harmonics generated by the pulses.

The PSOC implementation is shown in Figure 26:

Appendix A

Control Registers for a Type A Switched Capacitor Block

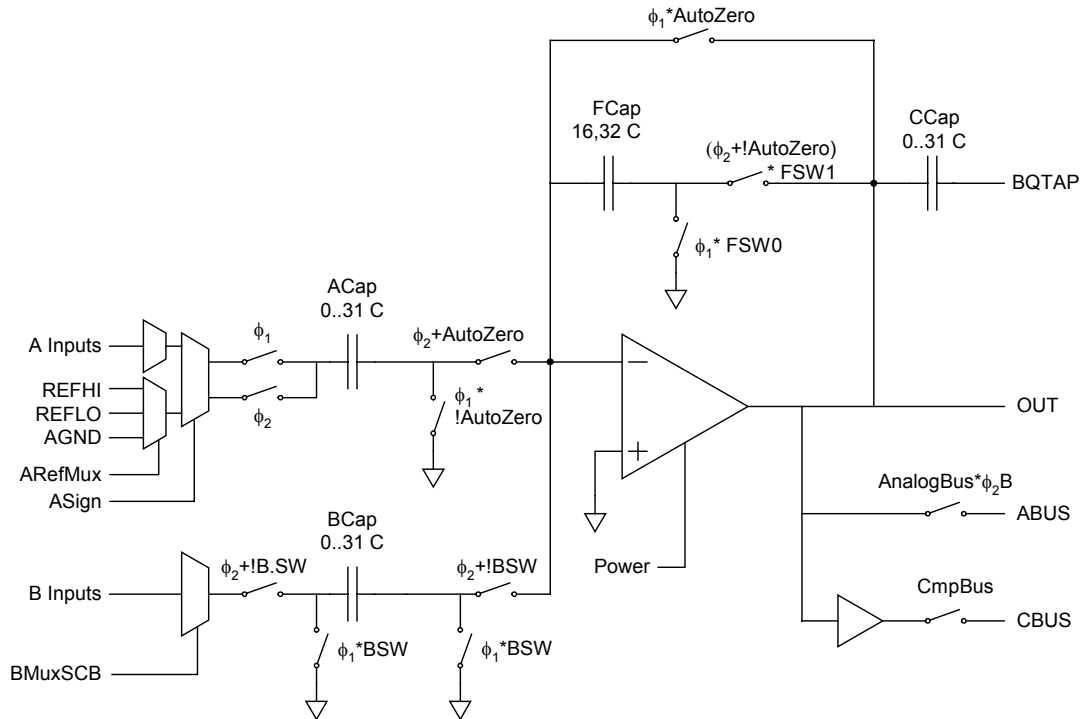
	7	6	5	4	3	2	1	0
CR0	FCap 16, 32	ClockPhase Norm, Swap	ASign Pos, Neg	ACap [0..31]				
CR1	ACMux C: North => A: North, E1W2, REFHI, South; C: Diag => A: Diag, Diag, Diag, Diag			BCap [0..31]				
CR2	AnalogBus Disable, Enable	CompBus Disable, Enable	AutoZero Off, On	CCap [0..31]				
CR3	ARefMux AGND, REFHI, REFLO, CMP		FSW1 Off, On	FSW0 Off, On	BMuxSCA North, E1W2, E2W1, South		Power Off, Low, Med, High	



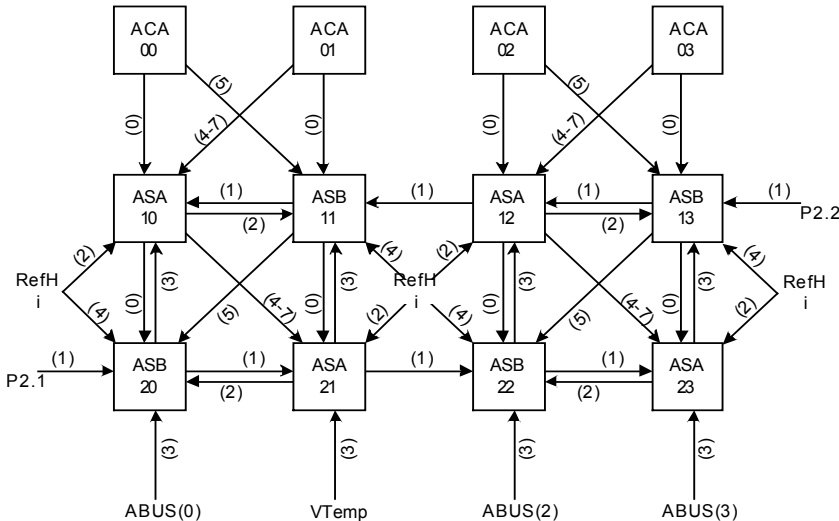
Appendix B

Control Registers for a Type B Switched Capacitor Block

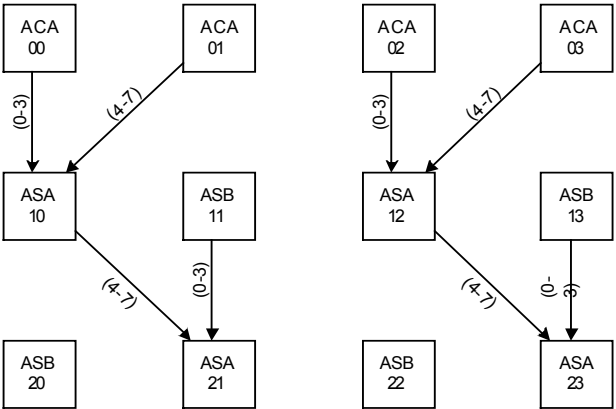
	7	6	5	4	3	2	1	0
CR0	FCap 16..32	ClockPhase Norm, Swap	ASign Pos, Neg	ACap [0..31]				
CR1	AMux North, E1W2, E2W1, South, REFHI, Diag, NC, Hold			BCap [0..31]				
CR2	AnalogBus Disable, Enable	CompBus Disable, Enable	AutoZero Off, On	CCap [0..31]				
CR3	ARefMux AGND, REFHI, REFLO, CMP		FSW1 Off, On	FSW0 Off, On	BSW Off, On	BMuxSCB Diag, North	Power Off, Low, Med, High	



Appendix C A Input Multiplexer Connections

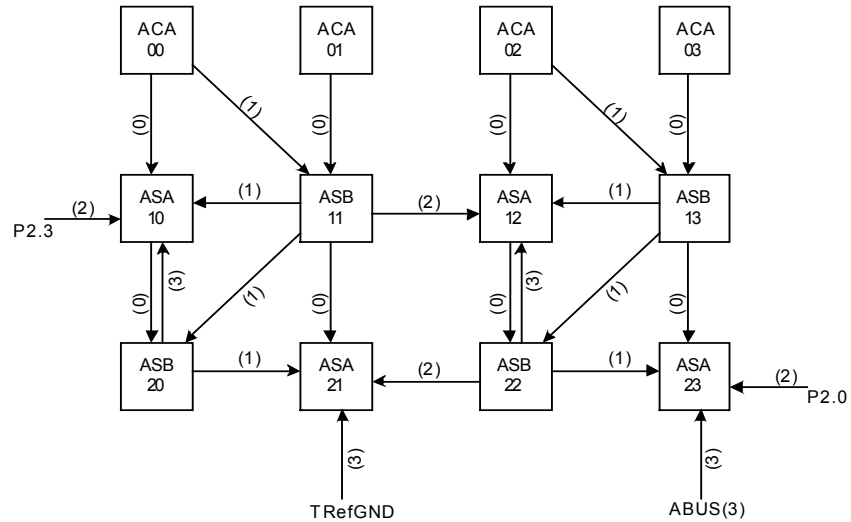


Appendix D C Input Multiplexer Connections



Appendix E

B Input Multiplexer Connections



Cypress MicroSystems, Inc.
 2700 162nd Street SW, Building D
 Lynnwood, WA 98037
 Phone: 800.669.0557
 Fax: 425.787.4641

<http://www.cypress.com/> / <http://www.cypress.com/support/mysupport.cfm>

Copyright © 2002-2004 Cypress MicroSystems, Inc. All rights reserved.

PSoC™ (Programmable System-on-Chip™) is a trademark of Cypress MicroSystems, Inc.

All other trademarks or registered trademarks referenced herein are property of the respective corporations.

The information contained herein is subject to change without notice.