

XRS10L620

PCI-X to 2-SATA/1-PATA
Host Controller



**PRELIMINARY
DATA SHEET**

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1. XRS10L620 Revision history

This document details the revision history for XRS10L620 and its derivatives as in Table1.

Table 1. Revision History

Release Day	Revision	Description	Notes
2008/09/29	0.10	Initial revision	

2. Overview

XRS10L620 is a 2ch-SATA 1ch-IDE controller with PCI-X interface. It can connect up to 4 devices at the same time, 2 SATA devices and 2 IDE/ATAPI devices. With its 32-bit PCI-X interface, it can easily with any MCU or CPU with PCI/PCI-X interface to form a powerful subsystem connecting high speed SATA storage devices and low cost IDE HD's and ODD's (optical disc drive).

The excellent compatibility of XRS10L620 with IDE HD's and ODD's make it especially suitable to construct an enclosure device with both IDE HD's and CD-ROM/DVD-ROM or CD/DVD burners, such as external SATA/IDE raid box or CD/DVD copy machine.

The two SATA channels on the chip can function in both HOST mode or TARGET mode. They comply with SATA Gen1 specification (Gen1 supports 1.5Gbps data rate). As for the IDE channel, the maximum transfer rate range from 16.7 MB/s to 150 MB/s. Further more, data transfer can take place among 3 devices to PCIX bus simultaneously.

3. Features

3-1 General

- 0.18um CMOS process technology
- Spread-Spectrum Clock (SSC) tolerance
- I²C interface operating in master/slave mode
- 2 SATA ports and 1 ATA/ATAPI port
- 1.8V/3.3V power supply
- 128-pin LQFP package

3-2 PCI-X Interface

- Compliant with PCI-X specifications Rev. 1.0a
- Compliant with PCI specification Rev 2.3
- Compliant with PCI Bus Power Management Interface Specification Rev 1.1
- 32bit PCI-X with burst data rate 400MB/s at 100MHz maximum.
- Supporting Dual Address Cycle (DAC), break the 4GB memory limit.
- Supporting Enhanced AHCI to reduce CPU overhead
- All registers appear in memory and IO space
- Flash ROM interface setup utility and booting

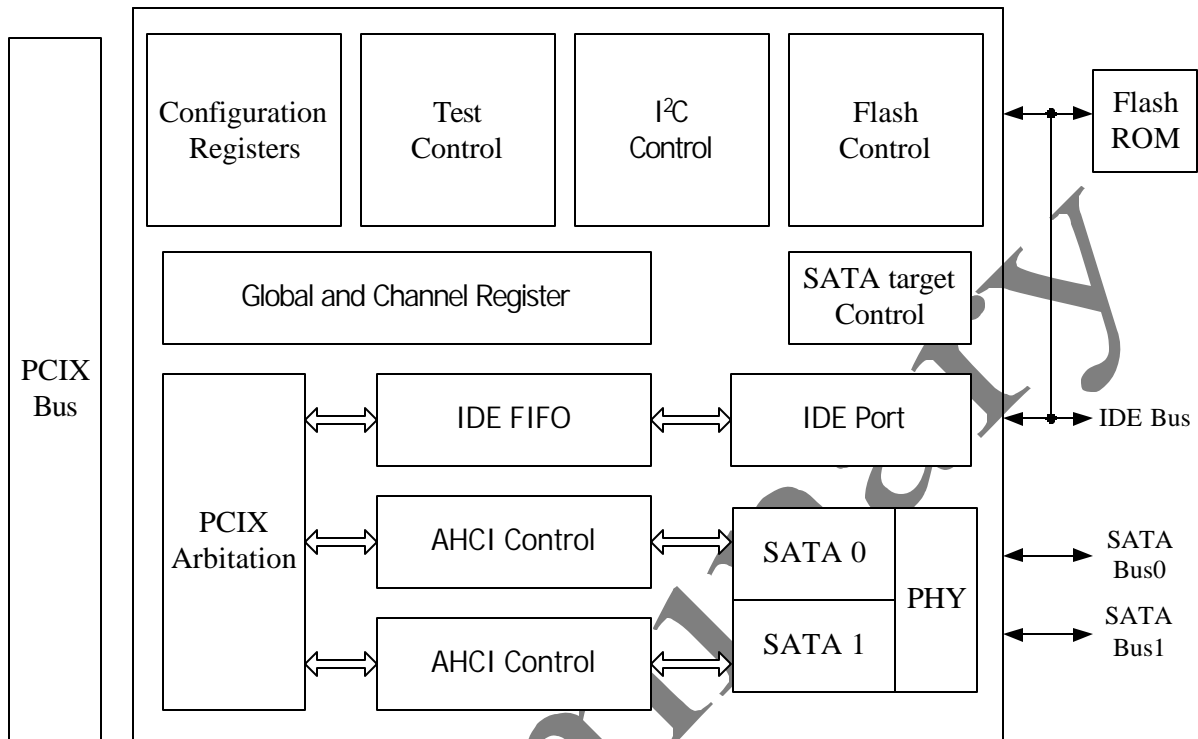
3-3 SATA Interface

- Conforming to Gen1i/Gen1m (1.5Gb/s), capable of eSATA
- Supporting 2 SATA ports with 1.5Gb/s data rate on each port
- Supporting Hot Plug for devices on channels or behind the Port Multiplier
- Supporting FIS-based switching (Port Multiplier 1.2)
- Supporting Asynchronous Notification
- Supporting Native Command Queuing (NCQ)
- Staggered spin-up control on 2 channels
- Individual device active LED indication
- I2C interface in master & slave role for SATA enclosure service
- Both ports can operate in TARGET mode, capable of processing NCQ commands

3-4 IDE Interface

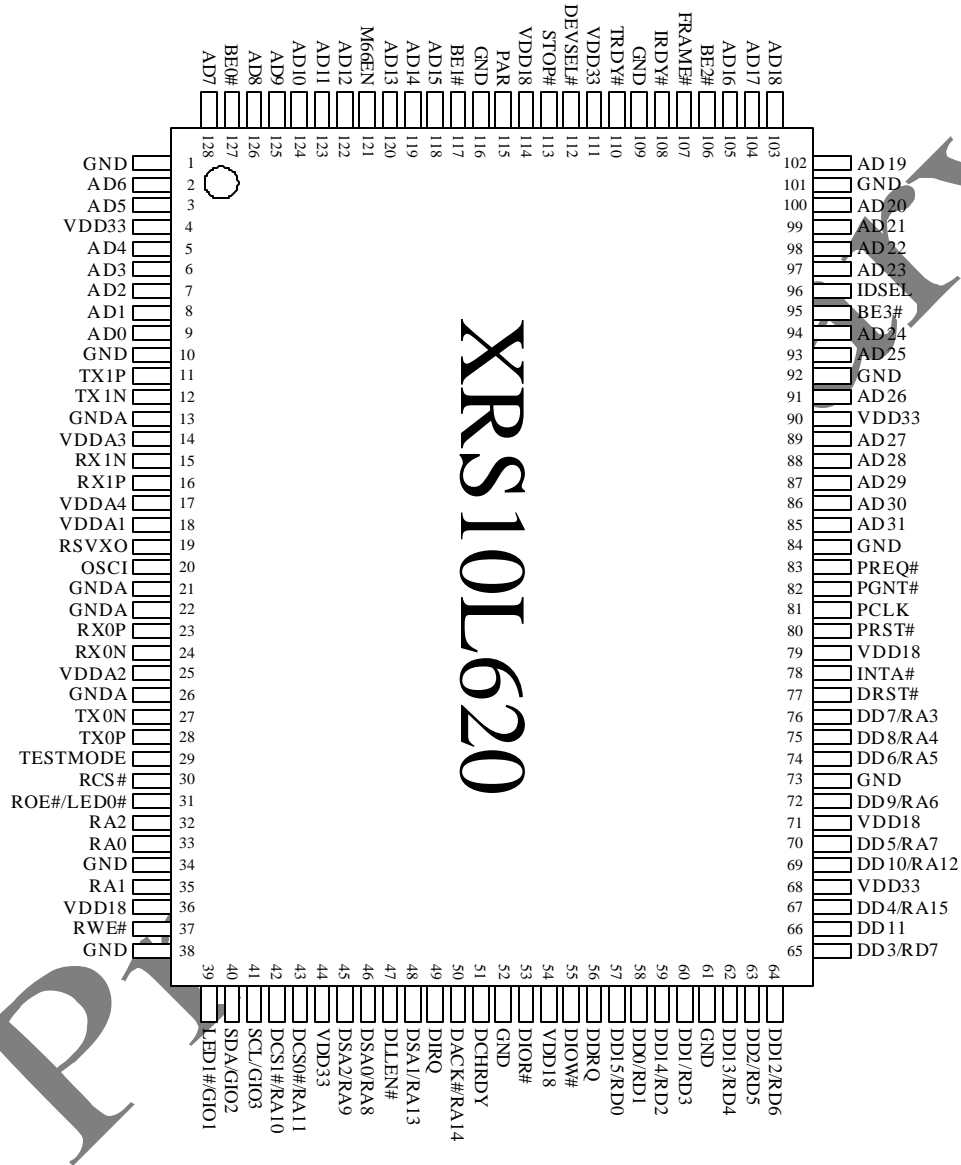
- One IDE channel to support master and slave devices
- Conforming to ATA-7 specification
- Supporting PIO mode 0, 1, 2, 3, 4 with 16.6MB/s data rate
- Supporting multiwordDMA mode 0, 1, 2 with 16.6MB/s data rate
- Supporting Ultra DMA mode 0, 1, 2, 3, 4, 5, 6 with data rate up to 150MB/s
- Programmable active and recovery cycle register timing per device

4. Block Diagram



5. PIN DIAGRAM

5.1 XRS10L620 128-pin Diagram





5.2 XRS10L620 Pin Assignment

Pin#	Name	I/O	Pin#	Name	I/O	Pin#	Name	I/O	Pin#	Name	I/O
1	GND		33	RA0	O/I	65	DD3/RD7	IO	97	AD23	IO
2	AD6	IO	34	GND		66	DD11	IO	98	AD22	IO
3	AD5	IO	35	RA1	O/I	67	DD4/RA15	IO	99	AD21	IO
4	VDD33		36	VDD18		68	VDD33		100	AD20	IO
5	AD4	IO	37	RWE#	O/I	69	DD10/RA12	IO	101	GND	
6	AD3	IO	38	GND		70	DD5/RA7	IO	102	AD19	IO
7	AD2	IO	39	LED1#/GIO1	IO	71	VDD18		103	AD18	IO
8	AD1	IO	40	SDA/GIO2	IO	72	DD9/RA6	IO	104	AD17	IO
9	AD0	IO	41	SCL/GIO3	IO	73	GND		105	AD16	IO
10	GND		42	DCS1#/RA10	O/I	74	DD6/RA5	IO	106	BE2#	IO
11	TX1P	O	43	DCS0#/RA11	O/I	75	DD8/RA4	IO	107	FRAME#	IO
12	TX1N	O	44	VDD33		76	DD7/RA3	IO	108	IRDY#	IO
13	GNDA		45	DSA2/RA9	O/I	77	DRST#	O	109	GND	
14	VDDA3		46	DSA0/RA8	O/I	78	INTA#	O	110	TRDY#	IO
15	RX1N	I	47	DLEN#	I	79	VDD18		111	VDD33	
16	RX1P	I	48	DSA1/RA13	O/I	80	PRST#	I	112	DEVSEL#	IO
17	VDDA4		49	DIRQ	I	81	PCLK	I	113	STOP#	IO
18	VDDA1		50	DACK#/RA14	O/I	82	PGNT#	I	114	VDD18	
19	RSVXO	O	51	DCHRDY	I	83	PREQ#	O	115	PAR	IO
20	OSCI	I	52	GND		84	GND		116	GND	
21	GNDA		53	DIOR#	O	85	AD31	IO	117	BE1#	IO
22	GNDA		54	VDD18		86	AD30	IO	118	AD15	IO
23	RX0P	I	55	DIOW#	O	87	AD29	IO	119	AD14	IO
24	RX0N	I	56	DDRQ	I	88	AD28	IO	120	AD13	IO
25	VDDA2		57	DD15/RD0	IO	89	AD27	IO	121	M66EN	I
26	GNDA		58	DD0/RD1	IO	90	VDD33		122	AD12	IO
27	TX0N	O	59	DD14/RD2	IO	91	AD26	IO	123	AD11	IO
28	TX0P	O	60	DD1/RD3	IO	92	GND		124	AD10	IO
29	TESTMODE	I	61	GND		93	AD25	IO	125	AD9	IO
30	RCS#	O/I	62	DD13/RD4	IO	94	AD24	IO	126	AD8	IO
31	ROE#/LED0#	O	63	DD2/RD5	IO	95	BE3#	IO	127	BE0#	IO
32	RA2	O/I	64	DD12/RD6	IO	96	IDSEL	I	128	AD7	IO

** O/I' : input function available only when PRST# active.

5.3 Pin Descriptions

● 5.3.1 PCI interface

Pin Name	Pin#	Type	Description
AD[31:0]	85-89,91,93,94, 97-100,102-105, 118-120,122-126, 128,2,3,5-9	I/O	PCI Multiplexed Address and Data
BE[3:0]#	95,106,117,127	I/O	PCI Command/Byte Enable
PAR	115	I/O	PCI Parity
FRAME#	107	I/O	PCI Cycle Frame
TRDY#	110	I/O	PCI Target Ready
IRDY#	108	I/O	PCI Initiator Ready
STOP#	113	I/O	PCI Stop
DEVSEL#	112	I/O	PCI Device Select
IDSEL	96	I	PCI Initialization Device Select
INTA#	78	O	PCI Interrupt Request A
PREQ#	83	O	PCI Master Request
PGNT#	82	I	PCI Master Grant
PCLK	81	I	PCI Clock
PRST#	80	I	PCI Reset
M66EN	121	I	PCI 66MHz indication

● 5.3.2 Serial ATA interface

Pin Name	Pin#	Type	Description
RSVXO	19	O	Reserved for internal test.
OSCI	20	I	External oscillator input. The clock rate is 25MHz, 1.8V level.
TX0P	28	O	SATA 0 positive output of the differential signal
TX0N	27	O	SATA 0 negative output of the differential signal
RX0N	24	I	SATA 0 positive input of the differential signal
RX0P	23	I	SATA 0 positive input of the differential signal
RX1P	16	I	SATA 1 positive input of the differential signal
RX1N	15	I	SATA 1 positive input of the differential signal
TX1N	12	O	SATA 1 negative output of the differential signal
TX1P	11	O	SATA 1 positive output of the differential signal

● 5.3.3 Parallel ATA interface

Pin Name	Pin#	Type	Description
DCS1#/RA10	42	O/I	IDE chip select 1
DCS0#/RA11	43	O/I	IDE chip select 0
DSA2/RA9	45	O/I	IDE address2
DSA0/RA8	46	O/I	IDE address0
DSA1/RA13	48	O/I	IDE address1
DIRQ	49	I	IDE interrupt
DACK#/RA14	50	O/I	IDE DMA acknowledge
DCHRDY	51	I	IO channel ready or DDSTROBE, DDMARDY#
DIOR#	53	O	IO read or HSTROBE, HDMARDY#
DIOW#	55	O	IO write or STOP
DD[15:0]	57,59,62,64, 66,69,72,75, 76,74,70,67, 65,63,60,58	I/O	IDE data bus
DRST#	77	O	IDE reset

● 5.3.4 Flash ROM pins (some are shared with IDE bus pins) :

Pin Name	Pin#	Type	Description
RCS#	30	O/I	ROM chip select
ROE#/LED0#	31	O/I	ROM output enable and SATA0 LED#
RWE#	37	O/I	ROM write enable
RA0	33	O/I	ROM address 0
RA1	35	O/I	ROM address 1
RA2	32	O/I	ROM address2
DD7/RA3	76	I/O	ROM address3
DD8/RA4	75	I/O	ROM address4
DD6/RA5	74	I/O	ROM address5
DD9/RA6	72	I/O	ROM address6
DD5/RA7	70	I/O	ROM address7
DSA0/RA8	46	O/I	ROM address8
DSA2/RA9	45	O/I	ROM address9
DCS1#/RA10	42	O/I	ROM address10
DCS0#/RA11	43	O/I	ROM address11

DD10/RA12	69	I/O	ROM address12
DSA1/RA13	48	O/I	ROM address13
DACK#/RA14	50	O/I	ROM address14
DD4/RA15	67	I/O	ROM address15
DD15/RD0	57	I/O	ROM data0
DD0/RD1	58	I/O	ROM data1
DD14/RD2	59	I/O	ROM data2
DD1/RD3	60	I/O	ROM data3
DD13/RD4	62	I/O	ROM data4
DD2/RD5	63	I/O	ROM data5
DD12/RD6	64	I/O	ROM data6
DD3/RD7	65	I/O	ROM data7

● **5.3.5 Miscellaneous :**

Pin Name	Pin#	Type	Description
LED1#/GIO1	39	I/O	SATA channel 1 LED and general IO pin
SDA/GIO2	40	I/O	I2C bus signal and general IO pin, internally pull up
SCL/GIO3	41	I/O	I2C bus signal and general IO pin, internally pull up
DLEN#	47	I	Internal test only
TESTMODE	29	I	Reserved, connected to GND normally

● **5.3.6 Power :**

Pin Name	Pin#	Type	Description
VDD18	36,54,71,79,114	1.8V	Digital 1.8V core power
VDD33	4,44,68,90,111	3.3V	Digital 3.3V IO power
VDDA4,VDDA3, VDDA2,VDDA1	17,14,25,18	1.8V	Analog 1.8V power supply. Each is connected to the series ferrite bead for noise suppression.
GND	1,10,34,38,52,61,73, 84,92,101,109,116		Digital ground, Each pin must have solid connection with PCB GND plane by at least 2 vias or other traces with it.
GNDA	13,21,22,26		Analog ground

● **5.3.7 Hardware configuration jumper setting :**

(All pins are pulled high or low in chip, 1 = pull high; 0 = pull low)

Pin Name	Pin#	Default	Description
RA1,RA0	35,33	1,1	PCI Device ID numbers : 1,1 = ' 000D' H 1,0 = ' 000E' H 0,1 = ' 000F' H 0,0 = ' 000D' H, reserved for internal test
RA2	32	1	0 = Enable staggered spin-up operation PCI-reset will not issue COMRESET to all SATA channels. HDDs spin-up are initiated by software 1= Disable staggered spin-up operation. PCI-reset will issue COMRESET to all SATA channels and spin up all SATA HDDs
DCS0#/RA11,	43	1	PCI SubClass number : 1= 00H (SCSI) 0= 04H(RAID)
DCS1#/RA10	42	1	Reserved for internal test. 1= fix phase
DSA1/RA13	48	1	Lowest address bit of I2C master (SEMB), high 6 bit = 101000B
DSA2/RA9	45	1	Both SATA channels TX driver initial level 0 = 500mV mode for Gen1i during initialization 1 = 550mV mode for Gen1m during initialization Other TX levels of each channel can be programmed by software
DSA0/RA8	46	1	1= forced Gen1 speed for SATA channel 0 0=Normal speed negotiation, for internal test only
RCS#	30	1	1= forced Gen1 speed for SATA channel 1 0=Normal speed negotiation, for internal test only
RWE#	37	1	1 = SATA0 is Host mode (default) 0 = SATA0 is Target mode
DACK#/RA14	50	1	1 = SATA1 is Host mode (default) 0 = SATA1 is Target mode

6. Register Definition

6.1 PCI Configuration Memory Registers :

(RWC : write 1 to clear)

(RW1 : write 1 to enable the bit and will be auto-cleared; write 0 has no function)

Addr	R/W	Name	Description
00,01	R	Vendor ID	1191h
02,03	R	Device ID	000Dh, 000Eh, 000Fh, depend on RA1,0 setting
04,05	RW	Command Register	Bit0 = 1 : enable IO space = 0: disable IO space Bit1 = 1 : enable Memory space = 0: disable Memory space Bit2 = 1 : enable Bus Master = 0: disable Bus Master Bit6 = 1 : enable Parity error response = 0: disable Parity error response Bit10 = 1 : disable INTA# = 0: enable INTA# Other bits are ' 0' , read only
06,07	R	Status Register	Bit3 = reflect the interrupt status Bit4 = 1 : with PCI power management capability Bit5 = 1 : 66 MHz capable Bit7 = 0 : Fast Back to Back Capable Bit8 = 1 : Data parity error detected by master Bit10,9 = 0,1 : medium DEVSEL timing Bit13 = 1 : Received Master abort Bit15 = 1 : Detected parity error by device
08	R	Revision ID	00h
09	R	Programming Interface	00h
0A	R	SubClass	00H (SCSI) or 04H(RAID), by DCS0#/RA11 configuration
0B	R	Basic Class	01h, mass storage
0C	RW	Cache Line Size	00h
0D	RW	Latency Timer	(00h, default) The register specify PCI clock count for this PCI master
0E	R	Header type	00h
0F	R	BIST	00h
10-13	RW	Base Addr Reg0	IO address of Global host & IDE registers, length 256 bytes bit0 : fixed to 1 bit[7:1] : fixed to 0 other bits are read/writable
14-17	RW	Base Addr Reg1	IO address of SATA channel 0 & 1 registers, length 256 bytes bit0 : fixed to 1 bit[7:1] : fixed to 0 other bits are read/writable
18-1B	RW	Base Addr Reg2	IO address reserved for test, length 256 bytes bit0 : fixed to 1

			bit[7:1] : fixed to 0 other bits are read/writable
1C-1F	RW	Base Addr Reg3	IO address reserved for test, length 256 bytes bit0 : fixed to 1 bit[7:1] : fixed to 0 other bits are read/writable
20-23	RW	Base Addr Reg4	IO address reserved for test, length 256 bytes bit0 : fixed to 1 bit[7:1] : fixed to 0 other bits are read/writable
24-27	RW	Base Addr Reg5	MEM address of Global and all SATA channels registers, length 1280 bytes. The Memory accessed registers are the same as those mapped by Base Addr [4:0]. bit[11:0] : fixed to 0, in 4KB range other bits are read/writable
28-2B	R	Card CIS Pointer	00000000h
2C-2F	R/W	Subsystem Vendor ID Subsystem Device ID	Default are same as Vendor ID and Device ID
30-33	R/W	Expansion ROM Base Address	bit0 : read/writable, set 1 to enable the ROM bit[15:1] : fixed to 0 bit[31:16] : read/writable
34	R	Cap_Pointer	(40h) point to power management link list
35-3B	R	Reserved	00h
3C	RW	Interrupt line	00h
3D	R	Interrupt pin	01h, INTA#
3E	R	Min_GNT	08h, specify a burst period in 250ns unit
3F	R	Max_LAT	0Dh, specify how often the device needs to gain access the PCI bus in 250ns unit
40 to 47	RW	PCI power management registers	Refer to section (2.1)
48 to 4F	RW	PCI-X Capabilities List Item	Refer to section (2.2)

6.1.1 PCI Power Management Registers :

CFGM+40h to 47h : 8 bytes PCI power management registers

CFGM+40h (R): Capability ID, default 01H

CFGM+41h (R): Next Item Pointer, default 48H

CFGM+42h,43h(R) : Power Management capabilities(PMC), default 0602H

CFGM+44h,45h(RW) : Power Management Control/Status Register(PMCSR)

Default 0000H

Bit [15:02]: all 0h, read only

Bit1,bit0 : Power State, read/write

00b is D0 state

01b is D1 state

10b is D2 state

11b is D3 hot state

CFGM+46h(R) : PMCSR_BSE register, default 00H

CFGM+47h(R) : Data register, default 00H

6.2 PCI-X Capabilities List Item :

CFGM+48h(R) : PCI-X capabilities ID, = 07h.

CFGM+49h(R) : Next Capability, = 00h

CFGM+4Ah(RW) : 16 bits PCI-X command register

Bit(s)	R/W	default	Description
15,14	R	00	Reserved PCI-X Capabilities List Item Version.
13,12	R	00	' 00' means Version 0, without ECC support and Capabilities List Item size is 8 bytes
11:7	R	00000	Reserved
6:4	RW	010	Maximum Outstanding Split Transactions. ' 010' means Maximum Outstanding at one time as a requester is 3. Values below ' 010' means 1 outstanding only. Other values are same as ' 010' .
3,2	RW	01	Maximum Memory Read Byte Count. ' 01' means Maximum byte count is 1024 for burst memory commands ' 00' means Maximum byte count is 512 for burst memory commands Other values are same as ' 01' .
1	R	0	Enable Relaxed Ordering ' 0' : The device never set the Relaxed Ordering attribute bit
0	RW	0	Uncorrectable Data Error Recovery Enable.

6.2.1 CFGM+4Ch(R) : 32 bits PCI-X Status Register

Bit(s)	R/W	default	Description
31	R	0	0 = PCI-X 533 not capable
30	R	0	0 = PCI-X 266 not capable (Not a PCI-X mode 2 device)
29	RWC	0	Received Split Completion Error Message. 0 = No Split Completion error message received. 1 = A Split Completion error message has been received.

28:26	R	010	Designed Maximum Cumulative Read Size ' 010' is 4KB(32 ADQs) cumulative outstanding when Maximum Memory Read Byte Count register is assigned to 1024 bytes. ' 001' is 2KB(16 ADQs) cumulative outstanding when Maximum Memory Read Byte Count register is assigned to 512 bytes.
25:23	R	010	Designed Maximum Outstanding Split Transactions. ' 010' means Maximum Outstanding at one time as a requester is 3.
22,21	R	01	Designed Maximum Memory Read Byte Count. ' 01' means Maximum byte count is 1024 for burst memory commands
20	R	0	Device Complexity 0 = simple device 1 = bridge device
19	RWC	0	Unexpected Split Completion 0 = No unexpected Split Completion has been received. 1 = An unexpected Split Completion has been received.
18	RWC	0	Split Completion Discarded. 0 = No Split Completion has been discarded. 1 = A Split Completion has been discarded.
17	R	1	1 = The device's maximum clock frequency is 133 MHz.
16	R	0	0 = The bus is 32 bits wide.
15:8	R	FFh	Bus Number. Each time the function is addressed by a Configuration Write transaction, it will update the register with the contents of AD[7:0] of the attribute phase of the Configuration Write.
7:3	R	1Fh	Device Number. Each time the function is addressed by a Configuration Write transaction, it will update the register with the contents of AD[15:11] of the attribute phase of the Configuration Write.
2:0	R	000	Function Number

6.3 Host Registers definition:

- (**IOG** = global, pointed by PCI Base Address Reg0)
- (**IO01** = channel0&1, pointed by PCI Base Address Reg1)
- (**IO23** = channel2&3, pointed by PCI Base Address Reg2, Reserved)
- (**IO45** = channel4&5, pointed by PCI Base Address Reg3, Reserved)
- (**IO67** = channel6&7, pointed by PCI Base Address Reg4, Reserved)
- (**MEM5** = pointed by PCI Base Address Reg5)

Register Table

Register addr	IO addr mapping	MEM addr mapping	Description
[13 : 00]	IOG+ [13 : 00]	MEM5+ [13 : 00]	AHCI generic host control
[7F : 14]	IOG+ [7F : 14]	MEM5+ [7F : 14]	Reserved
[9F : 80]	IOG+ [9F : 80]	NA	IDE channel registers
[FF : A0]	IOG+ [FF : A0]	MEM5+ [FF : A0]	I2C, GIO, PHY, Test registers
[17F : 100]	IO01+ [7F : 00]	MEM5+ [17F : 100]	AHCI SATA Channel 0 registers
[1FF : 180]	IO01+ [FF : 80]	MEM5+ [1FF : 180]	AHCI SATA Channel 1 registers

6.3.1 Global host registers : (IOG + 00h to 0FFh)
Reg_000H (IOG+00h) : Host Capability (CAP)

Bit(s)	R/W	default	Symbol	Description
31	R	1	S64A	Support 64-bit Addressing
30	R	1	SNCQ	Support Native Queue
29	R	0		Reserved
28	R	0	SIS	Support Interlock Switch
27	R	RA2 depends	SSS	1 = support Stagger Spin-up default =0, if RA2 pull up default =1, if RA2 pull down
26	R	0	SALP	Support Aggressive Link Power Management
25	R	1	SAL	Support Active LED
24	R	1	SCLO	Support Command List Override
23:20	R	0010	ISS	Interface Speed Support.
19	R	0	SNZO	Support Non-zero DMA offsets
18	R	1	SAM	Support AHCI mode only, no legacy mode
17	R	1	SPM	Support Port Multiplier, FIS base switching
16	R	0		Reserved
15	R	0	PMD	Only support single DRQ block data transfer for PIO
14	R	1	SSC	Slumber state capable
13	R	1	PSC	Partial state capable
12:08	R	11111	NCS	Support 32 command slots per channel
07:05	R	0		Reserved
04:00	R	00001	NP	Support maximum of 2 ports

Reg_004H (IOG+04h) : Global HBA Control (GHC)

Bit(s)	R/W	default	Symbol	Description
31	R	1	AE	Software can only access the chip using AHCI
30:02	R	0		Reserved
01	RW	0	IE	Interrupt Enable 0 = INTA# disabled for all interrupt from all ports 1 = INTA# enabled, if CFGM+4 bit10 =0 also

00	RW1	0	HR	HBA internal reset, issued by SW and auto-cleared when reset completed. SW should set ' 1' once for power on initialization. If Reg_000H bit 27(SSS)=0, COMRESET issued to all ports. If SSS=1, no COMRESET issued, SW need to spin-up each port after the reset has completed. The bit is self-cleared after reset action completed
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Reg_008H (IOG+08h) : Interrupt Status Register (IS)

Bit(s)	R/W	default	Symbol	Description
31	R	0	IFS	Interrupt flag when as I2C slave, means one byte received completed via I2C. Cleared when Reg_0B0H RXRS is read out
30	RWC	0	IFM	Interrupt flag when as I2C master, means one byte transfer completed via I2C. The interrupt is cleared as below : Master receive : Read out Reg_0B0H RXRM
29	RWC	0		Timer IRQ flag, 1=timer up Set 1 will clear this flag and timer IRQ signal (INTA#)
28:09	R	0		Reserved to 0
08	R	0	IDEPS	Latched IDE IRQ flag, reflect the Reg_090H bit 18 when Reg_090H bit 11 = 1
07:02	R	0		Reserved to 0
01:00	R	00b	IPS	If set, the corresponding bit map port has at least an interrupt flag in POIS, P1IS, and their POIE, P1IE are enabled respectively. Each bit is cleared when all flags in respective PxIS are cleared

Reg_00CH (IOG+0Ch): Ports Implemented

Bit(s)	R/W	default	Symbol	Description
31:02	R	0	PI	=1, the bit significant port is available.
01:00	R	11b		=0, the bit significant port is not available

Reg_010H (IOG+10h) : AHCI Version (VS)

Bit(s)	R/W	default	Symbol	Description
31:16	R	0001h	MJR	Major version is ' 1'
15:00	R	0000h	MNR	Minor version is ' 0'

Reg_014H to Reg_07FH are reserved.

Reg_080H to Reg_087H (IOG+80h to 87h) :

Reg_80h to 87h are mapped to standard Parallel IDE port 0 to port7

(The region is only IO port accessed, not available by memory access using MEM5 decoding)

Reg_088H to Reg_08DH (IOG+88h to 8Dh) : (RO)

Reserved to 00h

Reg_08EH (IOG+8Eh) :

Standard Parallel IDE alternate status and control register

Reg_08FH (IOG+8Fh) : (RO)

Reserved to 00h

Reg_090H (IOG+90h) : IDE DMA start/stop

Bit(s)	R/W	default	Description
31	RW	0	Test only for CH0 and CH1.
30:28	RW	000	FIFO threshold to initiate PCI write - request for IDE channel 000 : 7/8 FIFO full, 100 : 3/8 FIFO full 001 : 6/8 FIFO full, 101 : 2/8 FIFO full 010 : 5/8 FIFO full, 110 : 1/8 FIFO full 011 : 4/8 FIFO full, 111 : 1/8 FIFO full
27	R	0	Reserved
26:24	RW	000	FIFO threshold to initiate PCI read memory request for IDE channel 000 : 7/8 FIFO empty, 100 : 3/8 FIFO empty 001 : 6/8 FIFO empty, 101 : 2/8 FIFO empty 010 : 5/8 FIFO empty, 110 : 1/8 FIFO empty 011 : 4/8 FIFO empty, 111 : 1/8 FIFO empty
23:20	R	0000	Reserved for internal test
19	R	0	IDE FIFO ' NOT empty ' flag, 0 means empty
18	RWC	0	Latched IDE IRQ flag and also shown at Reg_008H bit8, fill 1 to clear the bit, or cleared when IDE IRQ is cleared.
17	RW	0	IDE IOR/W split enable, 1 = split enable
16	R	0	PCI/PCIX IDE DMA is active
15	RW	0	Set 1 to output low to reset IDE; 0 to normal state
14	RW	0	Set 1 to disable all IDE pins output
13	R	0	Reserved
12	R	0	Reserved for DLEN# pin
11	RW	0	1= enable IDE IRQ as PCI INTA# signal. Def ault 0=disable
10:8	R		PCI/PCIX mode indicator Bit 8 , 1= PCIX66 mode Bit 9 , 1= PCIX100 mode Bit 10 , 1= PCIX133 mode Bit (10,9,8)=(0,0,0) means PCI mode

7:4	R	00h	Reserved
3	RW	0	IDE DMA direction, 1 = write to host memory
2,1	R	00	Reserved
0	RW	0	Start/Stop PCI IDE DMA

Reg_094H (IOG+94h): IDE speed

Bit(s)	R/W	default	Description
31	R	0	Reserved
30,29,28	RW	000	Slave-IDE UDMA mode# +1, 000= disable UDMA, enable NDMA; 100= UDMA mode 3 001=UDMA mode 0 ; 101= UDMA mode 4 010= UDMA mode 1 ; 110= UDMA mode 5 011= UDMA mode 2 ; 111= UDMA mode 6
27	R	0	Reserved
26,25,24	RW	000	Master-IDE UDMA mode# +1, 000= disable UDMA, enable NDMA; 100= UDMA mode 3 001=UDMA mode 0 ; 101= UDMA mode 4 010= UDMA mode 1 ; 110= UDMA mode 5 011= UDMA mode 2 ; 111= UDMA mode 6
23	R	0	Reserved
22:20	RW	111	8 bit IDE ports speed, active cycles clocks (1 clk=26.7ns) 000 = 8 clk, 001=1 clk, ,110=6 clk, 111=12clk
19:16	RW	0000	8 bit IDE ports speed, recovery cycles clocks (1 clk=26.7ns) 0000= 12 clk, 0001=1 clk, ,1011=11 clk, 11xx=15clk
15	R	0	Reserved
14:12	RW	000	slave 16 bit IDE PIO/NDMA data active cycle clocks (1 clk=26.7ns) 000 = 8 clk, 001=1 clk, ,110=6 clk, 111=12clk
11:08	RW	0000	slave 16 bit IDE PIO/NDMA data recovery cycle clocks (1 clk=26.7ns) 0000= 12 clk, 0001=1 clk, ,1011=11 clk, 11xx=15clk
07	R	0	Reserved
06:04	RW	000	master 16 bit IDE PIO/NDMA data active cycle clocks (1 clk=26.7ns) 000 = 8 clk, 001=1 clk, ,110=6 clk, 111=12clk
03:00	RW	0000	master 16 bit IDE PIO/NDMA data recovery cycle clocks (1 clk=26.7ns) 0000= 12 clk, 0001=1 clk, ,1011=11 clk, 11xx=15clk

Reg_098H (IOG+98h) :

Low Dword address of Parallel IDE PRD pointer

Bit(s)	R/W	default	Description
31:02	RW	0	Low Dword address of Parallel IDE PRD pointer
01:00	R	0	Fixed to 0

Reg_09CH (IOG+9Ch) :

High Dword address of Parallel IDE PRD pointer

Bit(s)	R/W	default	Description
31:00	RW	0	High Dword address of Parallel IDE PRD pointer

Reg_0A0H (IOG+A0h) : Flash ROM data port

Access to the port will start ROM control signals 4 times, in/out the 8-byte ROM data bus with address bus defined in Reg_0A8H.

Bit(s)	R/W	default	Symbol	Description
31:24	RW			Flash ROM data port byte 3
23:16	RW			Flash ROM data port byte 2
15:08	RW			Flash ROM data port byte 1
07:00	RW			Flash ROM data port byte 0

Reg_0A4H (IOG+A4h) : GIO control

Bit(s)	R/W	default	Symbol	Description
31:30	RW	00		Function switch for GIO3 pin 00 = normal function, as SCL 01 = output user defined bit(bit23) to GIO3 10 = output one SATA channel debug signal to GIO3, see Reg_150H and Reg_1D0H 11 = output disabled, pure input mode Set 1 to negate other share pins function (like SCL, SDA, LED1Z, LED0Z), and dedicated as GIO pin(s)
29:28	RW	00		Function switch for GIO2 pin 00 = normal function, as SDA 01 = output user defined bit(bit22) to GIO2 10 = output one SATA channel debug signal to GIO2, see Reg_150H and Reg_1D0H 11 = output disabled, pure input mode Set 1 to negate other share pins function (like SCL, SDA, LED1Z, LED0Z), and dedicated as GIO pin(s)

27:26	RW	00	Function switch for GIO1 pin 00 = normal function, as LED1# 01 = output user defined bit(bit21) to GIO1 10 = output one SATA channel debug signal to GIO1, see Reg_150H and Reg_1D0H 11 = output disabled, pure input mode Set 1 to negate other share pins function (like SCL, SDA, LED1Z, LED0Z), and dedicated as GIO pin(s)
25:24	RW	00	Reserved
23:21	RW	000	User defined output value of GIO[3:1] pins, 1 to output high Available if modes in bit[31:26] are enabled respectively
20	RW	0	Reserved
19:17	R		GIO[3:1] pins input value respectively Available if modes in bit[31:26] are switched to input mode
16	R	0	Reserved
15	RW	0	1=GIO3 pin always output 1KHz signal when bit[31:30]=' 01'
14:01	R	0	Reserved
00	RW	0	Switch one SATA channel for output debug signals to GIO pin 0 = SATA channel 0 1 = SATA channel 1

Reg_0A8H (IOG+A8h) : PCI Bus Control and ROM Address

Bit(s)	R/W	default	Symbol	Description
31:18	RW	0		The corresponding RA[15:2] pins value, set 0/1 will output low/high, available if bit16(PIOROM) is enabled to ' 1' . Reading of the bits reflect the real pins value.
17	R	0		Reserved
16	RW	0		1=Enable PIOROM and also disable IDE function RA[15:2] output are controlled by bit [15:2] of this register RA[1:0] are auto-generated by chip
15:13	R	0		Reserved
12	RW	0		1= enable UDMA150, when Reg_094H is also set to UDMA mode 6 on that channel.
11	RW	0		Test only. 1= delayed write strobe
10	R/W	0		Test only, set 1 to disable DAC
09	RW	0		1 to issue DAC in every Memory access command, test only.

08	RW	0		0: Rolling PCI arbitration on all channels 1: Fixed PCI retry arbitration on all channels
07	R	0		M66EN pin value
06	RW	0		1 : Enable periodical issuing COMRESET on SATA channels when their PHY are not ready
05	RW	0		1 : For PCI-X, forced Memory Write command instead of Memory Write Block command
04	RW	0		Reserved
03	RW	0		1 : Disable Write SubSystem ID
02	RW	1		1 : Enable PCI burst
01	RW	1		1 : Enable PCI Memory Read Multiple
00	R	0		Reserved for PCI(X) 64 bit transfer

Reg_0ACH (IOG+ACh) : Timer Control

Bit(s)	R/W	default	Symbol	Description
31:24	R	0		Reserved
23,22	R	00		Test only, Mem1 result, ' 11' = good, other values= error
21:20	R	00		Test only, Mem0 result, ' 11' = good, other values= error
18	RW1	0	TSTM1	Test only. Start to test Mem1
17	RW1	0	TSTM0	Test only. Start to test Mem0
16	RW	0		1: Enable timer IRQ as INTA# signal
15	RW1	0		' 1' = start timer. The bit is auto-cleared when timer counts to 0
14:0	RW	0		15 bit timer count, in unit of 4 ms. Auto decrement to 0, when timer starts.

Reg_0B0H (IOG+B0h) : I2C Bus Control

Bit(s)	R/W	default	Symbol	Description
31:24	R	00h	RXRS	As Slave, last byte received via I2C
23:16	R	00h	RXRM	As Master, the byte content received via I2C
15:08	W		TXR	As Master, the byte content to transmit via I2C
07	W		STA	Generate START condition
06	W		STO	Generate STOP condition
05	W		RD	As Master, read from slave
04	W		WR	As Master, write to slave
03	W		AC	ACK, when as receiver, ' 0' to sent ACK, ' 1' sent NACK
02	RW		IFS	Enable interrupt flag (Reg_008H bit 31) to INTA# when as slave



01	RW		IFM	Enable interrupt flag (Reg_008H bit 30) to INTA# when as master
00	R		TIP	' 1' =Transfer In Progress; ' 0' =transfer complete

Reg_0B4H (IOG+B4h) : Reserved

Test only for 32 bit seed value

Reg_0B8H to Reg_0FFH (IOG+B8h to FFh) : Reserved

6.3.2 Port Registers (length 80h bytes per port/channel):

SATA Port 0 address = Reg_100H to Reg_17FH =(IO01+00h to 7Fh)

SATA Port 1 address = Reg_180H to Reg_1FFH =(IO01+80h to FFh)

Reg address from offset	Symbol	Description
00 – 03	PxCLB	Port x command list base address
04 – 07	PxCLBU	Port x command list base address upper 32bits
08 – 0B	PxFB	Port x FIS base address
0C – 0F	PxFBU	Port x FIS base address upper 32bits
10 – 13	PxIS	Port x interrupt status
14 – 17	PxIE	Port x interrupt enable
18 – 1B	PxCMD	Port x command
1C – 1F	PxPRBS40B_PAT	User defined pattern for internal test
20 – 23	PxTFD	Port x task file data
24 – 27	PxSIG	Port x signature
28 – 2B	PxSSTS	Port x SCR0: SStatus
2C – 2F	PxSCTL	Port x SCR1: Scontrol
30 – 33	PxSERR	Port x SCR2: Serror
34 – 37	PxSACT	Port x SCR3: Sactive
38 – 3B	PxCI	Port x command issue
3C – 3F	PxNOTIF	Port x Notification bits from devices behind P.Multiplier
40 – 43	PxCICLR	Clear Port x CI/SACT bits by host
44 – 47	PxSDBFG	32 Act bits of Set Device Bits FIS
48 – 5F		Registers for internal test
48 – 4B	PxDebug0	Debug port 0
4C – 4F	PxDebug1	Debug port 1
50 – 53	PxPHYCTRL	Physical Layer Control Register
54 – 57	PxPLLTEST	PLL Parameters
58 – 5B	PxTxTEST	Tx Parameters

5C – 5F	PxRxTEST	Rx Parameters
60 – 63	PxTFD1	MultiPM mode, Port x task file for Port Multiplier #1
64 – 67	PxTFD23	MultiPM mode, Port x task file for Port Multiplier #2,#3
68 – 6B	PxTFD45	MultiPM mode, Port x task file for Port Multiplier #4,#5
6C – 6F	PxTFD67	MultiPM mode, Port x task file for Port Multiplier #6,#7
70 – 73	PxAIS	Port x additional interrupt status, for PM #1 to 7
74 – 77	PxAIE	Port x additional interrupt enable, for PM #1 to 7
78 – 7B	PxAUFS	Port x Unknown FIS interrupt status and enable, for PM #1 to 7
7C – 7F		Reserved.

Reg_100H (IO01+00h) : P0CLB

Bit(s)	R/W	default	Symbol	Description
31:10	RW	0	CLB	Lower 32 bit base physical address of the command list, 1024 bytes aligned
09:00	R	0		Reserved

Reg_104H (IO01+04h) : P0CLBU

Bit(s)	R/W	default	Symbol	Description
31:00	RW	0	CLBU	Upper 32 bit base physical address of the command list

Reg_108H (IO01+08h) : P0FB

Bit(s)	R/W	default	Symbol	Description
31:08	RW	0	FB	Lower 32 bit base physical address of the received FISes, 256 bytes aligned
07:00	R	0		Reserved

Reg_10CH (IO01+0Ch) : P0FBU

Bit(s)	R/W	default	Symbol	Description
31:00	RW	0	FBU	Upper 32 bit base physical address of the received FISes

Reg_110H (IO01+10h) : P0IS, interrupt status

Bit(s)	R/W	default	Symbol	Description
31	R	0	CPDS	Cold detect status, reserved to 0
30	RWC	0	TFES	Task file error status 1 = error bit of status register is updated by the device and set.
29	RWC	0	HBFS	Host bus fatal error status 1 = PCI target or master abort

28	RWC	0	HBDS	Host bus data error status 1 = PCI parity error detected
27	RWC	0	IFS	Interface fatal error status 1 : The transfer is stopped due to SATA data FIS error
26	RWC	0	INFS	Interface non-fatal error status 1 = SATA non-data FIS error, but was able to continue by internal retry
25	RWC	0	UFSFG	Target mode only. Set ' 1 ' by HW when an unknown FIS is received to memory and no further FIS is received unless the bit is cleared by filling ' 1 ' from SW.
24	RWC	0	OFS	Overflow status HBA receive more bytes from a device than those in PRD
23	RWC	0	IPMS	Incorrect port multiplier status Always 0
22	R	0	PRCS	Reflect the value of PxSERR.N bit 1 = PhyRdy signal changed
21:17	R	0		Reserved
16:09	RWC	0		Represent PM# bit map, which has SDB FIS interrupt with ' I ' =1 and all 32 bits SACT are zero. Bit[16:9] map to PM#[7:0], while PM#[15:8] are overlapped in bit 9
08	R	0	NOTIS	' OR ' ed flag of 16 bits at Reg_13Ch bit[15:0]
07	R	0	DIS	Device interlock switch status, reserved to 0
06	R	0	PCS	Reflect the value of PxSERR.X bit 1 = new ComInit comes
05	RWC	0	DPS	Flag indicates all PRD data of a command table are transferred The bit is mandatory for Target mode to generate INTA#.
04:00		00000		If MultiPM bit (Reg_174H bit 1)=0, bit 4 and bit[2:0] fields are available for all PM#0 to #15 If MultiPM bit (Reg_174H bit 1)=1, bit 4 and bit[2:0] fields are dedicated for PM#0 only
04	R	0	UFS	Unknown FIS interrupt, when the FIS is copied to memory This bit is cleared by clearing PxSERR.DIAG..F bit
03	R	0	SDBS	' OR ' ed flag of 40 bits of this register bit[16:9] and Reg_144h[31:0] about Set Device Bits FIS interrupts
02	RWC	0	DSS	DMA setup FIS interrupt : This FIS is received with ' I ' bit set and has been copied into system memory

01	RWC	0	PSS	PIO setup FIS interrupt : This FIS is received with ' I' bit set, it and its related data are all transferred
00	RWC	0	DHRS	D2H register FIS interrupt : This FIS is received with ' I' bit set and has been copied into system memory

Reg_114H (IO01+14h) : POIE, interrupt enable of second layer

First layer enable are the CFGM+4 bit 10 and GHC.IE bit

Bit(s)	R/W	default	Symbol	Description
31	RW	0	CPDE	If set, INTA# issued when POIS.CPDS is set
30	RW	0	TFEE	If set, INTA# issued when POIS.TFES is set
29	RW	0	HBFE	If set, INTA# issued when POIS.HBFS is set
28	RW	0	HBDE	If set, INTA# issued when POIS.HBDS is set
27	RW	0	IFE	If set, INTA# issued when POIS.IFS is set
26	RW	0	INFE	If set, INTA# issued when POIS.INFS is set
25	R	0		Reserved
24	RW	0	OFE	If set, INTA# issued when POIS.OFS is set
23	RW	0	IPME	If set, INTA# issued when POIS.IPMS is set
22	RW	0	PRCE	If set, INTA# issued when POIS.PRCS is set ("N" bit)
21:09	R	0		Reserved
08	RW	0	NOTIE	If set, INTA# issued when POIS.NOTIS is set.
07	RW	0	DIE	If set, INTA# issued when POIS.DIS is set
06	RW	0	PCE	If set, INTA# issued when POIS.PCS is set ("X" bit)
05	RW	0	DPE	If set, INTA# issued when POIS.DPS is set (data completed)
04	RW	0	UFE	If set, INTA# issued when POIS.UFS is set (Unknown FIS)
03	RW	0	SDBE	If set, INTA# issued when POIS.SDBS is set
02	RW	0	DSE	If set, INTA# issued when POIS.DSS is set
01	RW	0	PSE	If set, INTA# issued when POIS.PSS is set
00	RW	0	DHRE	If set, INTA# issued when POIS.DHRS is set

Reg_118H (IO01+18h) : P0CMD, Port 0 control, capability and flag

Bit(s)	R/W	default	Symbol	Description
31:28	RW	0h	ICC	Interface communication control Host use the field to control SATA power management if the Link layer is in L_IDLE state, and no effect if not in the state Fh - 7h & 5h - 3h : Reserved 6h : HBA request a transition to the Slumber state 2h : HBA request a transition to the Partial state 1h : HBA request a transition to the Active state 0h : No-op/Idle. If software read this value, it is allowed to issue the above power management control. HBA will perform the above controls and update this field back to idle(0h).
27	R	0	ASP	Reserved for aggressive slumber /partial
26	R	0	ALPE	Reserved for aggressive link power management enable
25	RW	0	DLAE	Drive LED on ATAPI Enable 1=always drive LED regardless of PxCMD.ATAPI bit
24	RW	0	ATAPI	When set, the connected device of the port is an ATAPI
23	R	RWE#(0) RA14(1)	TGTZ	1=this SATA port is Host mode; 0=Target mode default value depend on RWE#(SATA0) or RA14(SATA1)
22:21	R	0		Reserved
20	R	0	CPD	0=Cold presence detection disable
19	R	0	ISP	Reserved to 0, 0= NOT support an interlock switch
18	R	1	HPCP	1=hot plug capable
17	RW	0	PMA	Port Multiplier attached, detected and set by software
16	R	0	CPS	Reserved
15	R	0	CR	Command list running, Indicates command list DMA engine of this port is running
14	R	0	FR	FIS receive running, Indicates FIS receive DMA engine of this port is running
13	R	0	ISS	Reserved
12:08	R	0	CCS	Current working command slot number in one of POCI
07:06	R	0		Reserved
05	RW	0		0 = normal reset level of ST (bit0) 1 = deeper reset level of ST, issue COMRESET on the channel
04	RW	0	FRE	FIS receive enable, ' 1 ' will post received FIS to host memory pointed by PxFB. Software must not set the bit until PxFB is a valid pointer.

03	RW1	0	CLO	Command list override, set the bit will clear PxTFD.STS.BSY and PxTFD.STS.DRQ so that software reset could be issued regardless BSY and DRQ bit value. The bit is auto-cleared to 0 when BSY & DRQ are cleared. Writing the bit with 0 has no effect. Host mode only, no effect on Target mode.
02	R	1	POD	Power on device, reserved to 1
01	RW	RA2	SUD	Spin-up device. Set and clear this bit by software. Writing the bit from 0 to 1 to issue COMRESET to the device Kept as ' 1' for normal operation
00	RW	0	ST	Start switch of command list DMA engine. Writing the bit from 0 to 1 starts processing from PxCI bit 0. Writing the bit from 1 to 0 will clear PxCI register. Different reset level is switched with bit5.

Reg_11CH (IO01+1Ch) : P0PRBS40B_PAT

User-defined pattern in PRBS check for internal test only.

Reg_120H (IO01+20h): P0TFD, Task file data of this port

The register copies specific fields of the task file when FISes are receive, like

- D2Hregister FIS
- PIO Setup FIS
- Set Device Bits FIS(not include BSY and DRQ bits)

For MultiPM bit (Reg_174H bit 1)= 0 :

The field is the received D2H Register FIS from all PM#0 to #15 devices, may be overlapped.

For MultiPM bit (Reg_174H bit 1)= 1 :

The field is the received D2H Register FIS from only PM#0 device, no overlap with other PM#.

Bit(s)	R/W	default	Symbol	Description
31:16	R	0h		Reserved
15:08	R	0h	ERR	Task file error register
07:00	R	7Fh	STS	Task file status register, with 3 bits that may affect AHCI Bit7 : BSY Bit3 : DRQ Bit0 : ERR

Reg_124H (IO01+24h) : P0SIG, signature of this port

For MultiPM bit (Reg_174H bit 1)= 0 :

The field is the received D2H Register FIS from all PM# devices, may be overlapped.

For MultiPM bit (Reg_174H bit 1)= 1 :

The field is the received D2H Register FIS from only PM#0 device, no overlap with other PM#.

Bit(s)	R/W	default	Symbol	Description
31:00	R	FFFF-FFFFh	SIG	Bit 31:24 : Cylinder high register (LBA [23:16]) Bit 23:16 : Cylinder low register (LBA [15:08]) Bit 15:08 : Sector number register (LBA [07:00]) Bit 07:00 : Sector count register

Reg_128H (IO01+28h) : POSSTS (SCR0 : SStatus)

Bit(s)	R/W	default	Symbol	Description
31:12	R	0		Reserved
11:08	R	0h	IPM	Indicates the current power state : 0h : Device not present or communication not established 1h : Active state 2h : Partial power management state 6h : Slumber power management state All other values reserved
07:04	R	0h	SPD	Indicates the negotiated speed. 0h : Device not present or communication not established 1h : Gen 1 rate negotiated 2h : Gen 2 rate negotiated All other values reserved
03:00	R	0h	DET	Device detection and Phy state 0h : No device detected and Phy not ready 1h : Device presence detected but Phy not ready 3h : Device presence detected and Phy ready 4h : Phy in offline since bus disabled or bus in a BIST loopback mode All other values reserved

Reg_12CH (IO01+2Ch) : P0SCTL (SCR2 : SControl)

Bit(s)	R/W	default	Symbol	Description
31:20	R	0h		Reserved
49:16	R	0h	PMP	Port Multiplier Port: not used by AHCI
15:12	R	0h	SPM	Select power management, not used by AHCI Use PxCMD.ICC instead
11:08	RW	0h	IPM	Indicates which power states are not allowed. 0h : No restrictions 1h : Disable transition to Partial state 2h : Disable transition to Slumber state 3h : Disable transition to both Partial and Slumber state All other values reserved
07:04	RW	0h	SPD	Indicates the highest allowable speed : 0h : No speed restriction 1h : Limit speed negotiation to Gen 1 2h : Limit fastest speed negotiation to Gen 2 All other values reserved

03:00	RW	0h	DET	<p>Control HBA's device detection and initialization.</p> <p>0h : No action requested</p> <p>1h : Perform initialization sequence like a hard reset.</p> <p>COMRESET is transmitted continuously until software change the field to 0h</p> <p>4h : Disable the SATA interface and put Phy in offline mode</p> <p>All other values reserved</p> <p>This field may only be modified when PxXMD.ST is ' 0' .</p>
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Reg_130H (IO01+30h) : POSERR (SCR1 : SError)

Bit(s)	R/W	default	Symbol	Description
31:16	RWC	0000h	DIAG	Diagnostics
31:27	R	0h		Reserved
26	RWC	0	X	Exchanged: 1=COMINIT(as Host) or COMRESET(as Device) received This bit is reflected in the POIS.PCS bit
25	RWC	0	F	Unknown FIS type received, include H2D and BIST FIS.
24	RWC	0	T	Transport state transition error
23	RWC	0	S	Link sequence error
22	RWC	0	H	Handshake error: R_ERR received, result from CRC, disparity, or 8b/10b error
21	RWC	0	C	CRC error
20	RWC	0	D	Disparity error: not used by AHCI
19	RWC	0	B	10b to 8b decode error
18	RWC	0	W	COMWAKE signal was detected by the Phy
17	RWC	0	I	Phy internal error
16	RWC	0	N	PhyRdy changed: This bit is reflected in POIS.PCRS bit
15:00	RWC	0000h	ERR	Error
15:12	R	0h		Reserved
11	RWC	0	E	Internal error: Master or Target abort occurred in the PCI bus
10	RWC	0	P	Protocol error: a violation of SATA protocol
9	RWC	0	C	Persistent communication error
8	RWC	0	T	Transient data integrity error: A data integrity error that was not recovered by the interface
7:2	R	0h		Reserved
1	RWC	0	M	Recovered communication error: Communication was temporarily lost between host and device.
0	RWC	0	I	Recovered data integrity error: A data integrity error occurred that was recovered by a retry operation.

Reg_134H (IO01+34h) : POSACT (SCR3 : SActive)

Bit(s)	R/W	default	Symbol	Description
31:00	RW1	0h	DS	Device status: used for FPDMA queuing operation prior to setting the PxCI.CI bit in the same command slot number. This field is clear via the Set Device Bits FIS, not by software.

Reg_138H (IO01+38h) : P0CI, Port0 command issue

Bit(s)	R/W	default	Symbol	Description
31:00	RW1	0h	CI	Set by software and cleared by hardware. Indicate that a command has been built for a command slot number. Cleared when the HBA receives a FIS with BSY, DRQ, and ERR bits cleared.

Reg_13CH (IO01+3Ch) : P0NOTIF (SCR4)

Bit(s)	R/W	default	Symbol	Description
31:28	R	0h	CLRPMP	Reserved
27:24	RW	0h	CLRPMP	The PM number for Reg_140H .CICLR to be cleared
23:16	R	0h	CLRPMP	Reserved
15:00	RWC	0h	NOTIF	Bit indication of Port Multiplier #15 to #0 ' 1 ' =this PM# receive a SetDevBits FIS with the N bit set to 1. The bit is cleared by SW writing ' 1 ' , but not cleared due to a COMRESET

Reg_140H (IO01+40h) : P0CICLR, Clear Port0 CI

Bit(s)	R/W	default	Symbol	Description
31:00	RW1	0h	CICLR	Force CI and SACT bits cleared by host Fill ' 1 ' to clear the respective CI/SACT bit, then the ' 1 ' will self-cleared to ' 0 ' . Only these CI bits belong to the same PM number can be cleared at a time. The PM# must be assigned at Reg_13FH bit[3:0] before this register is written

Reg_144H (IO01+44h) : POSDBFG

Bit(s)	R/W	Default	Symbol	Description
31:00	RWC	0h	SDBFG	Set by the 32 Act bits of Set Device Bits FIS Cleared by software when writing ' 1 ' to each bit

Reg_148H to Reg_15FH (IO01+48h to 5Fh) : Registers for internal test.

Addr	Name	Byte 3								Byte 2								Byte 1								Byte 0																																																																																																																					
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																																																																																																														
48h	Debug 0	ff_a2t_err	empty_t2a	emptu_a2t	link_state				ff_t2a_err	full_t2a	full_a2t	tp_state				0	crc_err		err_queue		0				0				fis_con_state																																																																																																																		
4Ch	Debug 1	0	empty_t2aC	emptu_a2t0	0				0	full_t2a0	0	0				0																																																																																																																															
50h	PHYCTRL	GIO3_SEL[3:0]								GIO2_SEL[3:0]								GIO1_SEL[3:0]								GIO0_SEL[3:0]								Reserved	FORCE15G	Reserved	Reserved	RXLOCKLLEN	PHYRDYCTRL	Reserved	PHYRSTI	PRBSALIGNLLEN	PRBSALIGNEN	PRBS40BPATEN	PRBS40BLEN	PRBS40BEN	FORCE3G	FORCEPHYRDY	PHYCTRLLEN																																																																																														
54h	PLLTEST	PLLTESTSEL				VFRSEL				PDPLL				LOCKDET				INDSEL				BYPASSLD				Reserved								Reserved								GIO3_SEL[5:4]				GIO2_SEL[5:4]				GIO1_SEL[5:4]				GIO0_SEL[5:4]																																																																																									
58h	TxTEST	PARTIAL		SLUMBER		TXRATE		Reserved								TXDRVLEVEL				Reserved								reserved	reserved	BYP_TXFIFO				Reserved								TXSTPATSEL				reserved	PRBSEN				PLPBKEN				SLPBKEN				PE				PDTX																																																																																
5Ch	RxTEST	PRBSOK / PRBSOKLL		RCVK28_5DET		PRBS40BOKLL		PRBSALIGNOK / PRBSALIGNOKLL								RX_LOCK / RX_LOCKLL				Reserved								RXRATE				CDR_CLKDP_DLY_EN				BLK_3RDDN_EN				UP2_EN				CDRCKOUT_SEL								CRCFHB								CRCFLB								PRBSOKLLEN								RXCRCBYP								CMMDETEN								CMMDETLHEN								BTALIGNEN								SQTHSEL								Reserved								DCDEN				PHFREEZE				EQ				SQLCHEMB				PDRX			

Reg_148H (IO01+48h): P0Debug_0

Bit(s)	R/W	Default	Symbol	Description
31:00	R		Debug_0	System Debug Port 0.

Reg_14CH (IO01+4Ch): P0Debug_1

Bit(s)	R/W	Default	Symbol	Description
31:00	R		Debug_1	System Debug Port 1.

Reg_150H (IO01+50h): P0PHYCTRL

Bit(s)	R/W	Default	Symbol	Description
31:28	RW	0000	GIO3_SEL	SEL[3:0], plus SEL[5:4] at Reg_154H bit [7:6], to select one of 64 sources to GIO3 pin output
SEL5,4= 0,0				00h : reserved 01h : COM_DET0 02h : COM_DET1 03h : DTAVLD0 04h : DTAVLD1 05h : RX_ERR (FIFO over flow) 06h : RX_LOCK 07h : DTA_UNDFLW (FIFO under flow) 08h : SIGLVD 09h : COMRSTINIT 0Ah : COMWAKE 0Bh : COMSAS 0Ch : PRBSOK 0Dh : RCVK28_5DET 0Eh : CDRCKOUT 0Fh : reserved
SEL5,4= 0,1				00h : PRBS40BOK 01h : PRBSALIGN_OK 02h : 0 03h : TXRATE_DFT 04h : RXRATE_DFT 05h : DEADCK_DET_DFT 06h : INVALID_DFT(8b/10b error) 07h : RDERR_DFT (disparity error) 08h : 0 09h : 0 0Ah : 0 0Bh : 0 0Ch : 0 0Dh : 0 0Eh : 0 0Fh : 0
SEL5,4= 1,0				00h : 0 01h : XPOUT_DFT[1] 02h : XPOUT_DFT[2] 03h : XPOUT_DFT[3] 04h : XPOUT_DFT[4] 05h : XPOUT_DFT[5] 06h : XPOUT_DFT[6] 07h : 0 08h : SELOUT_DFT[0] 09h : SELOUT_DFT[1] 0Ah : SELOUT_DFT[2] 0Bh : SELOUT_DFT[3] 0Ch : SELOUT_DFT[4] 0Dh : SELOUT_DFT[5] 0Eh : SELOUT_DFT[6] 0Fh : SELOUT_DFT[7]
SEL5,4= 1,1				Reserved to 0
27:24	RW	0000	GIO2_SEL	SEL[3:0], plus SEL[5:4] at Reg_154H bit [5:4], to select one of 64 sources to GIO2 pin output
23:20	RW	0000	GIO1_SEL	SEL[3:0], plus SEL[5:4] at Reg_154H bit [3:2], to select one of 64 sources to GIO1 pin output
19:16	RW	0000		Reserved

15	R	0		Reserved.
14	RW	RA8	FORCE1.5G	0 = normal 1 = fixed at 1.5G mode, never changed to 3G during negotiation
13:12	R	00		Reserved.
11	RW	0	RXLOCKLL_EN	when RX input signal > squelch threshold level and RX is locked, Reg_5CH bit 27 is high. Once the signal is going low, this bit is latched to low
10	RW	0	PHYRDY_CTRL	
9	R	0		Reserved.
8	RW	0	PHYRSTI	Set 1 to reset PHY, 0 to restore.
7	RW	0	PRBSALIGNLLEN	Transmit/check Align primitive with error latched to a low flag
6	RW	0	PRBSALIGNEN	Transmit/check Align primitive
5	RW	0	PRBS40BPATEN	Transmit/check Dword pattern specified in Reg_1CH.
4	RW	0	PRBS40BLEN	Enable 40 bit PRBS or defined pattern transmit/check with error latched to a low flag
3	RW	0	PRBS40BEN	Enable 40 bit PRBS transmit/check
2	RW	0	FORCE3G	1=Fixed at 3G mode, never changed to 1.5G during speed negotiation
1	RW	0	FORCEPHYRDY	0: Normal operation. 1: Forced PHY ready regardless OOB power on initialization.
0	RW	0	PHYCTRLLEN	Set 1 to control TXrate, RXrate, Slumber, Partial function

Reg_154H (IO01+54h): P0PLLTEST

** P1PLLTEST(IO01+D4h) is reserved, not available.

Bit(s)	R/W	Default	Symbol	Description
31:29	RW	000	PLLTESTSEL	Select different PLL test mode 000= Test mode disabled 100= Bandgap voltage 001= Vcoin voltage 101= Charge pump current source 010= Ground voltage 110= Charge pump current sink 011= Vddreg voltage 111= VCO free running
28:26	RW	111	VFRSEL	Select Vcoin free running voltage 111 = 1.5V 011 = 1.0V 110 = 1.4V 010 = 0.9V 101 = 1.3V 001 = 0.7V 100 = 1.2V 000 = 0.5V
25	RW	0	PDPLL	1 = Power down PLL 0 = Normal operation
24	R	1	LOCKDET	1 = PLL is locked 0 = PLL is not locked

23:21	RW	000	INDSEL	3 bits to select one of the signals below as 'COM_DET0 name shown in Reg_50H bit [19:16] 000 = COMDET0/CMMDETLH0 100 = COMSAS 001 = PRBSOK/PRBSOKLL 101 =SQUCH 010 = COMINIT 110 = reserved 011 = COMWAKE 100 = reserved
20	RW	0	BYPASSLD	Bypass LOCKDET 1=POR_DG does not wait for LOCKDET (POR_DG=POR when BYPASSLD=1) 0=POR_DG waits for LOCKDET
19:08	R	0		Reserved
7:6	RW	0	GIO3_SEL	GIO3_SEL[5:4], see also Reg_150H bit[31:28]
5:4	RW	0	GIO2_SEL	GIO2_SEL[5:4], see also Reg_150H bit[27:24]
3:2	RW	0	GIO1_SEL	GIO1_SEL[5:4], see also Reg_150H bit[23:20]
1:0	RW	0		Reserved

Reg_158H (IO01+58h) : P0TxTEST
****bit [15:6] of P1TxTEST (IO01+D8h) are reserved**

Bit(s)	R/W	Default	Symbol	Description
31	RW	0	PARTIAL	Power down TX and RX in Partial mode 1 = Power down 0 = No power down Read value is from SATA return value
30	RW	0	SLUMBER	Power down TX and RX in Slumber mode 1 = Power down 0 = No power down Read value is from SATA return value
29	RW	1	TXRATE	1 = TX in 3G mode 0 = TX in 1.5G mode Read value is from SATA return value
28:24	R	0		Reserved
23,22	RW	RA9, 0	TXDRVLEVEL	Select different TX driver levels 0,0= 500mV mode for Gen1i 0,1= 1000mV mode for proprietary use 1,0= 550mV mode for Gen1m 1,1= 1200mV mode for Gen1x
21:18	R	0		Reserved
17,16	R	00		Reserved
15	RW	0	BYP_TXFIFO	Bypass TX FIFO 1 = Bypass 0 = No Bypass
14:12	R	0		Reserved

11:08	RW	0000	TXTSTPATSEL	Select different TX test patterns 0000=disabled 0001=IDLE 0100=High frequency pattern 0101=Low frequency pattern 0110=Mixed frequency pattern 0111=Alternate K28.3 pattern 1000=ALIGN 1001=COMINIT generation 1010=COMWAKE generation 1011=COMSAS generation
7	R	0		Reserved
6	RW	0	PRBSEN	Enable PRBS generation(TX) and checking(RX) 1 = Enable PRBS 0 = Disable PRBS
5	RW	0	PLPBKEN	Far-End Retimed Loopback 1 = TX/RX in Far -end loopback 0= TX/RX not in Far -end loopback
4	RW	0	SLPBKEN	Enable Near-End analog Loopback 1 = TX/RX in Near-End loopback 0= TX/RX not in Near-End loopback
3:1	RW	000	PE	Control pre-emphasis level 000 = no pre-emphasis ... 111=strongest pre-emphasis
0	RW	0	PDTX	1 = Power down TX 0 = Not power down TX

Reg_15CH (IO01+5Ch) : P0RxTEST
****bit [21:8] of P1RxTEST (IO01+DCh) are reserved**

Bit(s)	R/W	Default	Symbol	Description
31	R	1	PRBSOK / PRBSOKLL	Switched by PRBSOKLLEN(bit15) 1 = PRBS OK 0 = PRBS error
30	R	0	CMMDETLH	Comma detection latching high signal
29	R	1	PRBS40BOK / PRBS40BOKLL	Switched by PHYCTRL=>PRBS40BLL_EN(bit4) 1 = PRBS40B OK 0 = PRBS40B error
28	R	1	PRBSALIGNOK / PRBSALIGNOKLL	Switched by PHYCTRL=>PRBSALIGNLL_EN(bit6) 1 = PRBSALIGN OK 0 = PRBSALIGN error
27	R	1	RX_LOCK / RX_LOCKLL	Switched by PHYCTRL=>RX_LOCKLL_EN(bit11) 1 = RX input signal > squelch threshold level and RX is locked 0 = RX input signal < squelch threshold level or RX is not locked
26	R	0		Reserved
25	RW	1	RXRATE	1 = RX in 3G mode 0 = RX in 1.5G mode Read value is from SATA return value
24	RW	0	UP2_EN	Reserved
23	RW	1	BLK_3RDDN_EN	Reserved

22	RW	0	CDR_CLKDP_DLY _EN	Reserved
21:20	RW	00	CDRCKOUT_SEL	Select different CDRCKOUT clock frequency For Gen1 : 00=disabled 01=37.5MHz 10=75MHz 11=150MHz For Gen2 : 00=disabled 01=75MHz 10=150MHz 11=300MHz
19:18	RW	01	CRCFHB	RX FIFO upper threshold 00= 12 01=13 10=14 11=15
17:16	RW	01	CRCFLB	RX FIFO lower threshold 00= 4 01=5 10=6 11=7
15	RW	0	PRBSOKLLEN	Select PRBSOK latching low enable 1 = Enable latching low for PRBSOK 0 = Disable latching low for PRBSOK
14	RW	0	RXCRCBYP	Bypass RX Clock Rate Compensation FIFO 1 = Bypass 0 = No Bypass
13	RW	1	CMMDETEN	1 = Enable comma detector in RX 0 = Disable comma detector in RX
12	RW	0	CMMDETLHEN	Enable to select comma detection latching high 1 = Enable comma detection latching high 0 = Disable comma detection latching high
11	RW	1	BTALIGNEN	1 = Enable byte alignment for comma detector 0 = Disable byte alignment for comma detector
10:8	RW	000	SQTHSEL	Control squelch threshold voltage levels 000 = normal 100 = +20 % 001 = -10 % 101 = +40 % (for SAS) 010 = -20 % 110= reserved 011 = +10 % 111= reserved
7:6	R	00		Reserved
5	RW	1	DCDEN	Dead(CDR Recovered) Clock Detection Enable 1 = Enable 0 = Disable
4	RW	0	PHFREEZE	Freeze phase selection of phase interpolator. 1 = Freeze phase 0 = Normal mode
3:2	RW	11	EQ	Control RX equalizer level 00 = no equalization ... 11 = strongest equalization
1	RW	0	SQLCHENB	Squelch circuit enable signal 0 = Enable squelch circuit 1 = Disable squelch circuit
0	RW	0	PDRX	1 = Power down RX lane 0 = Not power down RX lane

Reg_160H to Reg_16FH (IO01+60h to 6Fh) :

Port 0 Task File registers for Port Multiplier #1 to #7

These fields are valid only when Reg_174H bit 1 (P0MultiPM) is ' 1' for FIS-based switching

Reg_160H (IO01+60h) : PxTFD1 for PM# 1

Bit(s)	R/W	default	Symbol	Description
31:24	R	0h	ERR1	PortX, PM#1 Task file error register
23:16	R	7Fh	STS1	PortX, PM#1 Task file status register, with BSY, DRQ, ERR bits

15:08	R	0h	ERRF	PortX, PM#F Task file error register
07:00	R	0h	ST SF	PortX, PM#F Task file status register, with BSY, DRQ, ERR bits

Reg_164H (IO01+64h) : PxTFD23 for PM# 2,3

Bit(s)	R/W	default	Symbol	Description
31:24	R	0h	ERR3	PortX, PM#3 Task file error register
23:16	R	7Fh	STS3	PortX, PM#3 Task file status register, with BSY, DRQ, ERR bits
15:08	R	0h	ERR2	PortX, PM#2 Task file error register
07:00	R	7Fh	STS2	PortX, PM#2 Task file status register, with BSY, DRQ, ERR bits

Reg_168H (IO01+68h): PxTFD45 for PM# 4,5

Bit(s)	R/W	default	Symbol	Description
31:24	R	0h	ERR5	PortX, PM#5 Task file error register
23:16	R	7Fh	STS5	PortX, PM#5 Task file status register, with BSY, DRQ, ERR bits
15:08	R	0h	ERR4	PortX, PM#4 Task file error register
07:00	R	7Fh	STS4	PortX, PM#4 Task file status register, with BSY, DRQ, ERR bits

Reg_16CH (IO01+6Ch): PxTFD67 for PM# 6,7

Bit(s)	R/W	default	Symbol	Description
31:24	R	0h	ERR7	PortX, PM#7 Task file error register
23:16	R	7Fh	STS7	PortX, PM#7 Task file status register, with BSY, DRQ, ERR bits
15:08	R	0h	ERR6	PortX, PM#6 Task file error register
07:00	R	7Fh	STS6	PortX, PM#6 Task file status register, with BSY, DRQ, ERR bits

Reg_170H to Reg_17FH (IO01+70h to 7Fh) :
Port 0 Additional Interrupt Status and Enable for PM # 1 to 7

These fields are valid only when Reg_174H bit 1 (P0MultiPM) is ' 1' for FIS-based switching

Reg_170H (IO01+70h) : P0AIS, Port 0 Additional Interrupt Status

Bit(s)	R/W	default	Symbol	Description
31:28	RWC	0h		Bit 31: Reserved Bit 30: PM#7 DMA Setup FIS received interrupt flag Bit 29: PM#7 PIO Setup FIS received interrupt flag Bit 28: PM#7 D2H Register FIS received interrupt flag
27:24	RWC	0h		Bit 27: Reserved Bit 26: PM#6 DMA Setup FIS received interrupt flag Bit 25: PM#6 PIO Setup FIS received interrupt flag Bit 24: PM#6 D2H Register FIS received interrupt flag

23:20	RWC	0h	Bit 23: Reserved Bit 22: PM#5 DMA Setup FIS received interrupt flag Bit 21: PM#5 PIO Setup FIS received interrupt flag Bit 20: PM#5 D2H Register FIS received interrupt flag
19:16	RWC	0h	Bit 19: Reserved Bit 18: PM#4 DMA Setup FIS received interrupt flag Bit 17: PM#4 PIO Setup FIS received interrupt flag Bit 16: PM#4 D2H Register FIS received interrupt flag
15:12	RWC	0h	Bit 15: Reserved Bit 14: PM#3 DMA Setup FIS received interrupt flag Bit 13: PM#3 PIO Setup FIS received interrupt flag Bit 12: PM#3 D2H Register FIS received interrupt flag
11:08	RWC	0h	Bit 11: Reserved Bit 10: PM#2 DMA Setup FIS received interrupt flag Bit 09: PM#2 PIO Setup FIS received interrupt flag Bit 08: PM#2 D2H Register FIS received interrupt flag
07:04	RWC	0h	Bit 07: Reserved Bit 06: PM#1 DMA Setup FIS received interrupt flag Bit 05: PM#1 PIO Setup FIS received interrupt flag Bit 04: PM#1 D2H Register FIS received interrupt flag
03	RW	0h	PM#F D2H Register FIS received interrupt flag
02:00	RW	0h	Reserved

Reg_174H (IO01+74h) : P0AIE, Port 0 Additional Interrupt Enable

Similar to P0IE, first layer enable is CFGM+4 bit 10 and GHC.IE bit

Bit(s)	R/W	default	Symbol	Description
31:28	RW	0h		Bit 31: reserved Bit 30: If set, INTA# issued when P0AIS bit 30=1 for PM#7 Bit 29: If set, INTA# issued when P0AIS bit 29=1 for PM#7 Bit 28: If set, INTA# issued when P0AIS bit 28=1 for PM#7
27:24	RW	0h		Bit 27: reserved Bit 26: If set, INTA# issued when P0AIS bit 26=1 for PM#6 Bit 25: If set, INTA# issued when P0AIS bit 25=1 for PM#6 Bit 24: If set, INTA# issued when P0AIS bit 24=1 for PM#6
23:20	RW	0h		Bit 23: reserved Bit 22: If set, INTA# issued when P0AIS bit 22=1 for PM#5 Bit 21: If set, INTA# issued when P0AIS bit 21=1 for PM#5 Bit 20: If set, INTA# issued when P0AIS bit 20=1 for PM#5
19:16	RW	0h		Bit 19: reserved Bit 18: If set, INTA# issued when P0AIS bit 18=1 for PM#4 Bit 17: If set, INTA# issued when P0AIS bit 17=1 for PM#4 Bit 16: If set, INTA# issued when P0AIS bit 16=1 for PM#4
15:12	RW	0h		Bit 15: reserved Bit 14: If set, INTA# issued when P0AIS bit 14=1 for PM#3 Bit 13: If set, INTA# issued when P0AIS bit 13=1 for PM#3 Bit 12: If set, INTA# issued when P0AIS bit 12=1 for PM#3

11:08	RW	0h		Bit 11: reserved Bit 10: If set, INTA# issued when P0AIS bit 10=1 for PM#2 Bit 09: If set, INTA# issued when P0AIS bit 09=1 for PM#2 Bit 08: If set, INTA# issued when P0AIS bit 08=1 for PM#2
07:04	RW	0h		Bit 07: reserved Bit 06: If set, INTA# issued when P0AIS bit 06=1 for PM#1 Bit 05: If set, INTA# issued when P0AIS bit 05=1 for PM#1 Bit 04: If set, INTA# issued when P0AIS bit 04=1 for PM#1
03	RW	0		If set, INTA# issued when P0AIS bit 03=1 for PM#F
02	RW	0	PassD2H	' 1 ' will always receive D2H FIS independent of BSY, DRQ bit value
01	RW	0	MultiPM	Enable multiple PM devices FIS-based switching, for PM#0 to 7 and #F only. It should be disabled for other PM#, the PM#8 to #E.
00	RW	0	NCQSW	Enable NCQ

Reg_178H (IO01+78h) : P0AUFIS, additional unknown FIS interrupt status & enable

Bit(s)	R/W	default	Symbol	Description
31	RWC	0h		Target mode only. Set when an illegal NCQ tag# is received, cleared by filling from SW
30:29	R	0h		Reserved
28:24	RW	0h		Target mode only, the maximum queue tag#. Any tag# of NCQ command is illegal if larger than the number
23	R	0		Reserved
22:20	RW	0		FIFO threshold to request PCI write memory from SATA0 000 = 7/8 FIFO full 001 = 6/8 FIFO full 010 = 5/8 FIFO full 011 = 4/8 FIFO full 100 = 3/8 FIFO full 101 = 2/8 FIFO full 110 = 1/8 FIFO full 111 = 1/8 FIFO full
19	R	0		=1 when main FIFO is non-empty
18:16	RW	0		FIFO threshold to request PCI read memory to SATA0 000 = 7/8 FIFO empty 001 = 6/8 FIFO empty 010 = 5/8 FIFO empty 011 = 4/8 FIFO empty 100 = 3/8 FIFO empty 101 = 2/8 FIFO empty 110 = 1/8 FIFO empty 111 = 1/8 FIFO empty



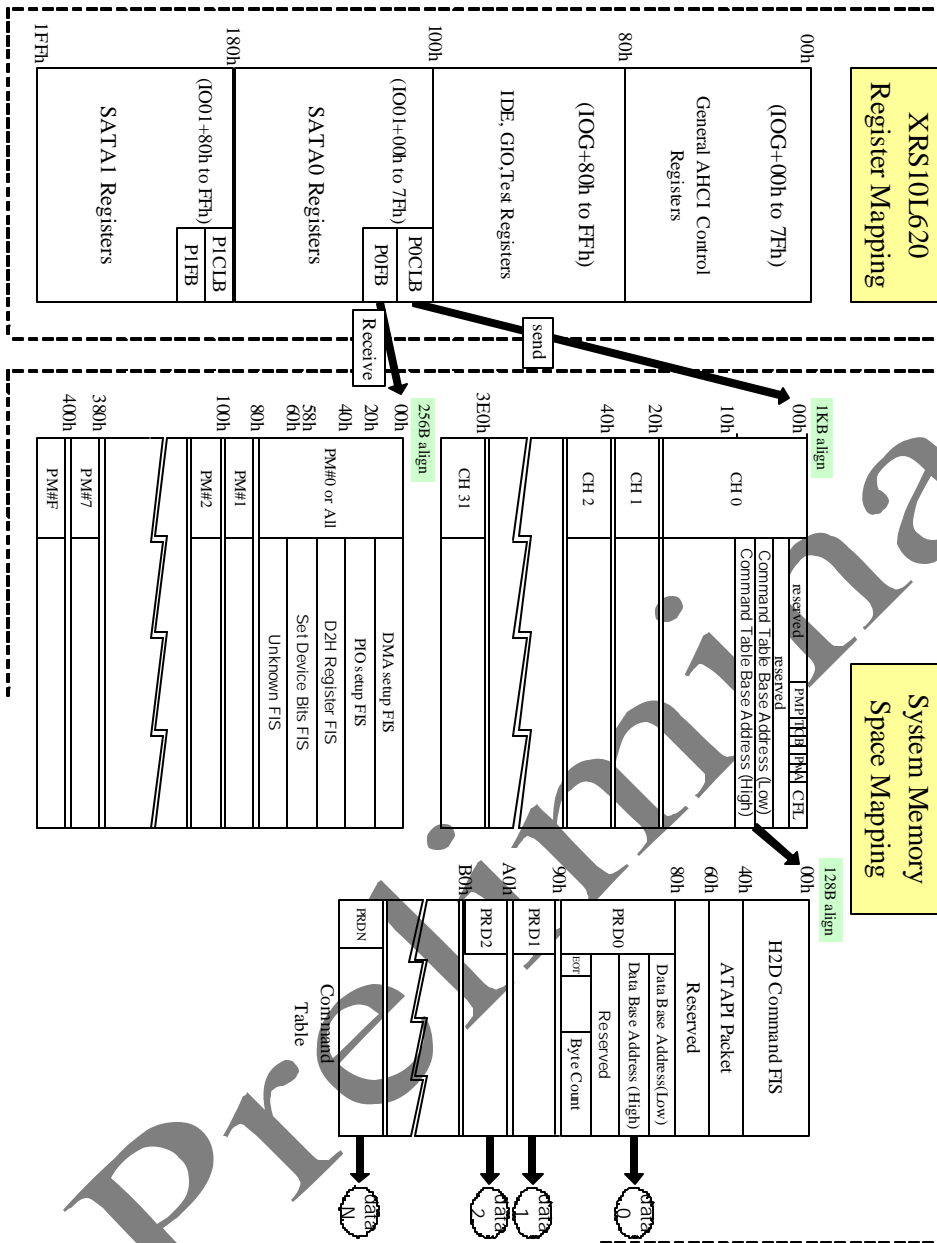
15:08	RW	0h	Bit 15: enable PM#7 Unknown FIS received interrupt Bit 14: enable PM#6 Unknown FIS received interrupt Bit 13: enable PM#5 Unknown FIS received interrupt Bit 12: enable PM#4 Unknown FIS received interrupt Bit 11: enable PM#3 Unknown FIS received interrupt Bit 10: enable PM#2 Unknown FIS received interrupt Bit 09: enable PM#1 Unknown FIS received interrupt Bit 08: reserved
07:00	RWC	0h	Bit 07: PM#7 Unknown FIS received interrupt flag Bit 06: PM#6 Unknown FIS received interrupt flag Bit 05: PM#5 Unknown FIS received interrupt flag Bit 04: PM#4 Unknown FIS received interrupt flag Bit 03: PM#3 Unknown FIS received interrupt flag Bit 02: PM#2 Unknown FIS received interrupt flag Bit 01: PM#1 Unknown FIS received interrupt flag Bit 00: reserved

Reg_17CH to Reg_17FH (IO01+7Ch to 7Fh) :
Reserved.

Preliminary

7. System Memory Structure

Fig. 6.1 XRS10L620 register and system memory mapping



7.1 Received FIS structure

The structure is in the system memory and pointed in unit of 256 bytes by PxFB, as shown in Fig. 6.1.

Each Port Multiplier has 80h memory space. The XRS10L620 support 8 PM numbers, PM#0 to PM#7, at the same time with FIS-base switching. Higher Port Multiplier numbers like PM#8 to PM#14, can be connected also under Command-base switching.

The Unknown FIS include the H2D FIS and BIST FIS.

7.2 Command List Structure

Total 32 Command Headers are defined with 4-DW(16 bytes) each that details the direction, type, and scatter/gather pointer of the command. The Command List is aligned in 1024 bytes.

Further details of each field are listed below.

DW#	Bit#	Description
DW0	31:16	Reserved
	15:12	Port Multiplier Port(PMP): Indicates the port number that should be used when constructing data FISes on transmit, and to check against all FISes received for this command.
	11	Data phase flag. Set to one for Target mode only when Data FIS is transferred.
	10	Clear Busy upon R_OK(C): When set, the HBA shall clear PxTFD.STS.BSY and PxCI bit after transmitting this FIS and receive R_OK, no need to wait the relative D2H FIS. Host mode : Set to one for first H2D FIS of soft reset sequence Target mode : Set to one for all non -Data FIS transmitting to the host.
	09	BIST(B): reserved
	08	Reserved
	07	Prefetchable(P): When set, the HBA will prefetch 8 more PRDs during Data FIS transfer. The bit is not available if NCQSW or MultiPM bits are enabled(PxAIE bit1,0)
	06	Write(W): When set, the direction is device write (data from system memory to device)
	05	ATAPI(A): When set, indicates a PIO setup FIS shall be sent by the device indicating a transfer for the ATAPI packet.
	04:00	Command FIS Length(CFL): Length of the Command FIS, in DW.
DW1	31:00	Reserved
DW2	31:07	Command Table Base Address(Low):low 32 bits physical address pointer to the command table that is 128-byte aligned
	06:00	Reserved
DW3	31:07	Command Table Base Address(High):high 32 bits physical address pointer.
	06:00	Reserved

7.3 Command Table and PRD table

The table contains the command FIS, ATAPI Command, and PRD table as shown in Fig6.1.

It is aligned in 128 bytes.

The Command FIS field contains the H2D FIS to be sent to the device, or any FISes to be sent to the host when as Target mode. The DWord count is same as CFL field in Command Header.

The ATAPI Packet field contains either 12 or 16 bytes to transmit if ' A' bit is set in the Command Header.

The PRD table format is as below :

DW#	Bit#	Description
DW0	31:00	Data Base Address(Low)
DW1	31:00	Data Base Address(High)
DW2	31:00	Reserved
DW3	31	End of Transfer(EOT): indicates the last PRD of the whole list
	30:17	Reserved
	16:00	Byte count of this PRD, 64KB(10000h) maximum

8. Target mode Programming Note

All kinds of non-Data FIS can be sent out through ' H2D Command FIS' field in Command Table.

The incoming command (H2D FIS) is received to the ' Unknown FIS' field of the Receive FIS region, in company with an interrupt and flag to remind the host CPU to handle it.

Hardware can accept one H2D FIS each time with a flag set in PxIS bit 25, the software need to clear this flag for next receiving FIS.

To transfer Data FIS, the software need to prepare the PRD tables, set the ‘ T ’ bit and fill the direction bit ‘ W ’ in CH0. Only one Command Header (CH0) and one Received FIS (PM#0) are used for all Target mode operations, even in NCQ commands handling.

Except for the first 2 bytes, other contents in CH0 are the same for all Data and non-Data FISes. The reserved field are filled with zero, the command table base address are filled to point to command table.

The following table lists all FISes available for Target mode.

	FIS	First 2 bytes of CH0	Note
1	Register-D2H	05h, 04h, ...	
2	DMA Setup	07h, 04h, ...	
3	Set Device Bits	02h, 04h, ...	
4	BIST Activate	03h, 04h, ...	
5	PIO Setup (data from memory)	05h, 04h, ...	
6	PIO Data, from memory	4xh, 08h, ...	
7	PIO Data, to memory (included PIO Setup)	05h, 08h, ...	5 Dword PIO Setup FIS in the Command Table
8	DMA Data, from memory	4xh, 08h, ...	
9	DMA Data, to memory (included DMA Activate)	01h, 08h, ...	1 Dword DMA Activate FIS in the Command Table

9. PCB High-Speed Layout Design Guidelines

1. High speed differential signals (TX+ & TX-, RX+ & RX-) should be routed as micro-strips on layer 1. No via or stubs for these critical traces. Differential pairs trace length should be identical.
2. Impedance should be controlled at 100 ohms +- 5% for differential pair, and 50 ohms +- 10% for single ended.
3. Keep the trace length of differential pairs as short as possible. Avoid sharp turns, use rounded corner. It is highly recommended to keep them within two inches long. Make sure no other signals are routed near these critical traces. Keep

a good separation between these differential pairs and other signals, minimum of 50 mils clearance is recommended.

4. Recommended board stack-up and routing example:

Material: FR4, with Dielectric constant of 4.2, and total thickness 62 mils.

	Thickness	Diff Pair Width	Diff Pair Spacing
Layer 1, Signal	0.5 oz	8 mils	12 mils
FR4 Prepreg	4 mils		
Layer 2, Ground	1 oz		
FR4 Prepreg	47 mils		
Layer 3, Power	1 oz		
FR4 Prepreg	4 mils		
Layer 4, Signal	0.5 oz		

5. When the differential layout cannot be achieved, e.g. around the connector area, neck-down technique to maintain single-ended 50 ohms is highly recommended.
6. For other signals where VIA is unavoidable, anti-pad is required to provide adequate clearance.
7. Place AC coupled 10nF capacitors as close as possible to the connector end, minimize the soldering pad area. The layout of capacitors can be combined with SATA connector to minimize impedance discontinuities. Use smaller footprint like 0402 to minimize package parasitic.
8. Use surface mount SATA connector, avoid over-soldering. Minimize the width of RX and TX soldering pads for SATA connector.
9. Separate analog power island on top layer for VDDA1, VDDA2, VDDA3, etc... via used to connect to the ferrite bead should be placed close to device power pins.
10. It is recommended that Analog power supplies VDDA should be isolated from the core VDD1.8V power plane through a noise suppression ferrite bead, which should provide 30dB or more attenuation for frequency less than 650 MHz.
11. Put decoupling capacitors with value of both 0.1uF and 0.01uF after ferrite bead. Place all decoupling capacitors as close to the device pins as possible.
12. A Ground plane should be on layer 2, the Ground plane should be solid underneath the high speed differential pairs to provide good return path.
13. Put enough Ground stitches throughout the board.
14. Each digital ground pin (GND) must have solid connection with PCB GND plane by at least 2 vias or other traces with it.
15. Signals should avoid crossing the split power planes. If have to, add some bypass capacitors across the split planes. For example, if some signals across 1.8V and 3.3V planes on the adjacent layer, then put a 0.1uF capacitor connecting 1.8V and 3.3V near the signals.

10. Electrical Characteristics

Specifications are for Commercial Temperature range, 0°C to +70°C, unless otherwise specified.

10.1 Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
VDD33	I/O Supply Voltage	3.7	V
VDD18	Core Supply Voltage	1.9	V
VDDA	Analog Supply Voltage	1.9	V
Vin	Input Voltage	-0.3 ~ VDD33+0.3	V
Tstg	Storage Temperature	-55 ~ 125	°C
HBM	ESD capability – HBM	2000	V
MM	ESD capability - MM	200	V

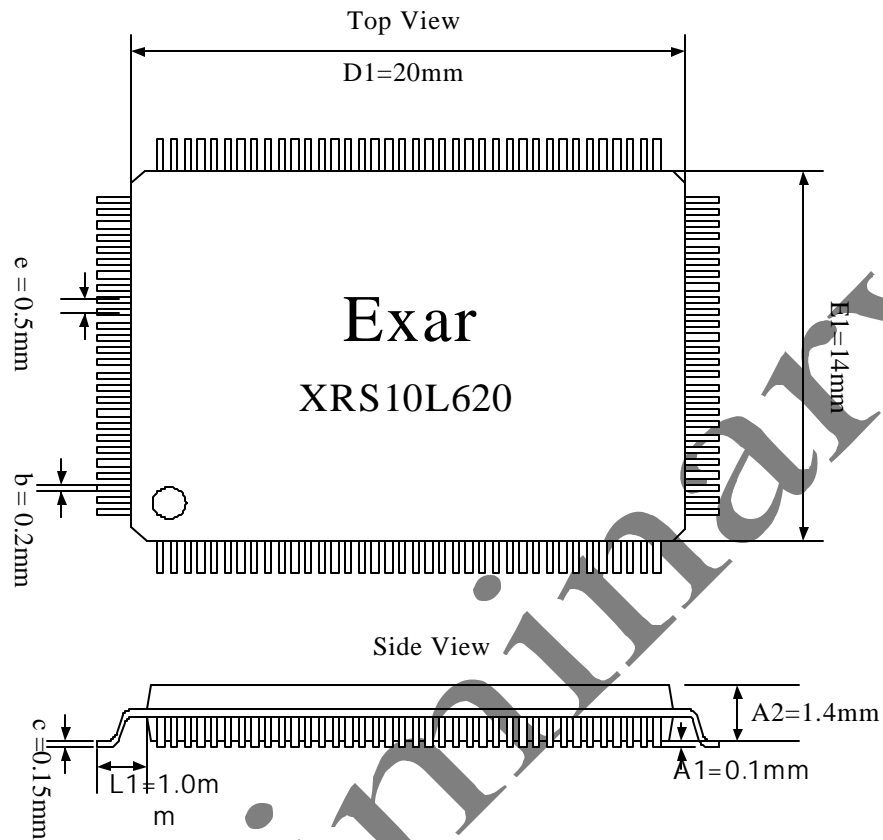
10.2 Typical Operating Condition

Parameter	Min.	Typ.	Max.	Unit	Note
Operating Temperature	-10		70	°C	
Digital IO (VDD33)	3.14	3.3	3.63	V	
Digital Core (VDD18)	1.71	1.8	1.98	V	
SATA PHY (VDDA)	1.71	1.8	1.98	V	

10.3 DC Specifications

Parameter	Min.	Typ.	Max.	Unit	Note	
Digital IO (IDD33)	SATA1.5G	4.6	55	60	mA	Min.=idle Typ.=Read/Write at PCI 66MHz Max.=Read/Write at PCIX 100MHz (SATA 3G is for internal test only.)
	SATA3G	7.6	55	60	mA	
Digital Core (IDD18)	SATA1.5G	118	170	190	mA	Condition as IDD33.
	SATA3G	118	220	245	mA	(SATA 3G is for internal test only.)
SATA PHY (IDDA)	SATA1.5G	125	125	126	mA	Condition as IDD33. All VDDA1,2,3,4 current.
	SATA3G	125	140	142	mA	(SATA 3G is for internal test only.)
Input low voltage (Vil)			0.9	V		
Input high voltage (Vih)	2.0			V		
Output low voltage (Vol)			0.4	V	Io= 8mA	
Output high voltage (Voh)	2.4			V	Io= -8mA	
Weak pull high resistance	39	47	116	KΩ		

11. Package Dimension



12. Appendix

12.1 Product ordering information



12.1.1 IC Marking Information

XRS10L620 LQFP 128 pin

TBD

12.1.2 Product Ordering Information

X	R	S	1	0	L	6	2	0	C
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Valid Combinations

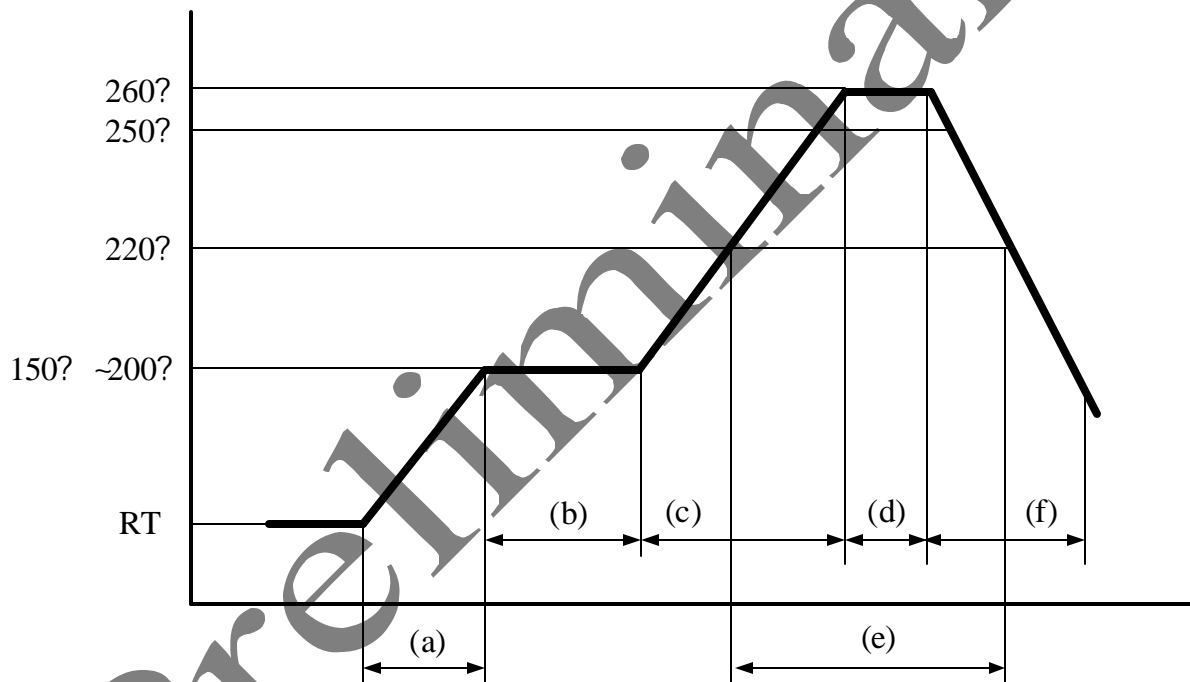
XRS10L620 CV-F

Preliminary

12.2 Soldering temperature profile

- (a) Temp. inc gradient: Avg. 1~4? /sec.
- (b) Preliminary heating: Temp.150~200? /sec., 70~150? /sec.
- (c) Temp. inc. gradient: Avg. 1~3? /sec.
- (d) Actual heating: Temp. 260? max
250? up 20sec max
- (e) Temp.220? up 40~70sec.
- (f) Cooling: Natural Cooling or Forced Cooling

***Package Surface Temp.**



13. Application Circuit

Preliminary